11.10 PIO output AC specification

Reference clock in this case means the last transition of any PIO signal.

Note: There are two different sets of PIO timings, one for the SSC (I2C) outputs and one for all other PIO outputs.

Figure 30: PIO output waveforms

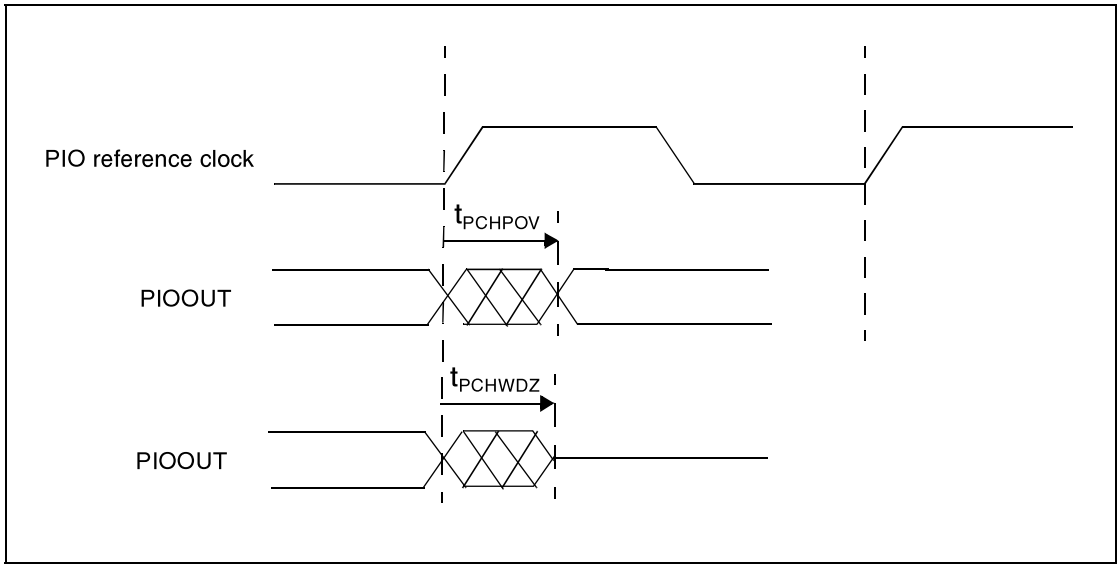


Table 59: PIO SSC output AC timings

Symbol	Parameter	Min	Max	Units
t_{PCHPOV}	PIO_REFCLOCK high to PIO output valid	-20.0	0.0	ns
t_{PCHWDZ}	PIO tristate after PIO_REFCLOCK high	-20.0	5.0	ns
t_{PIOr}	Output rise time	3.0	30.0	ns
t_{PIOf}	Output fall time	3.0	30.0	ns

Table 60: PIO other outputs AC timings

Symbol	Parameter	Min	Max	Units
t_{PCHPOV}	PIO_REFCLOCK high to PIO output valid	-6.0	0.0	ns
t_{PCHWDZ}	PIO tristate after PIO_REFCLOCK high	-6.0	5.0	ns
t_{PIOr}	Output rise time	1.0	7.0	ns
t_{PIOf}	Output fall time	1.0	7.0	ns

11.11 MAFE interface output AC specification

Input clock: MAFE_SCLK (PIO2(7) when selected

Outputs: MAFE_HC1 (PIO2[3]), MAFE_DOUT (PIO2[4])

Figure 31: MAFE interface output waveforms

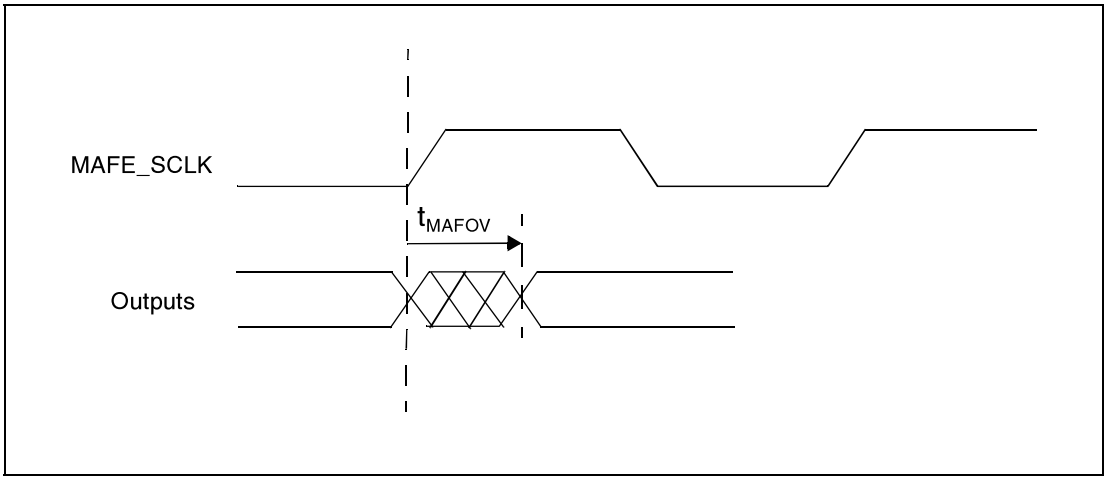


Table 61: MAFE interface output timings

Symbol	Parameter	Min	Max	Units
Input clock	MAFE_SCLK clock period		100	ns
t_{MAFOV}	Output delay to MAFE_CLK		20	ns

11.12 MAFE interface input AC specification

Input clock: MAFE_SCLK (PIO2[7]) when selected

Outputs: MAFE_DIN (PIO2[5]), MAFE_FS (PIO2[6])

Figure 32: MAFE interface input waveforms

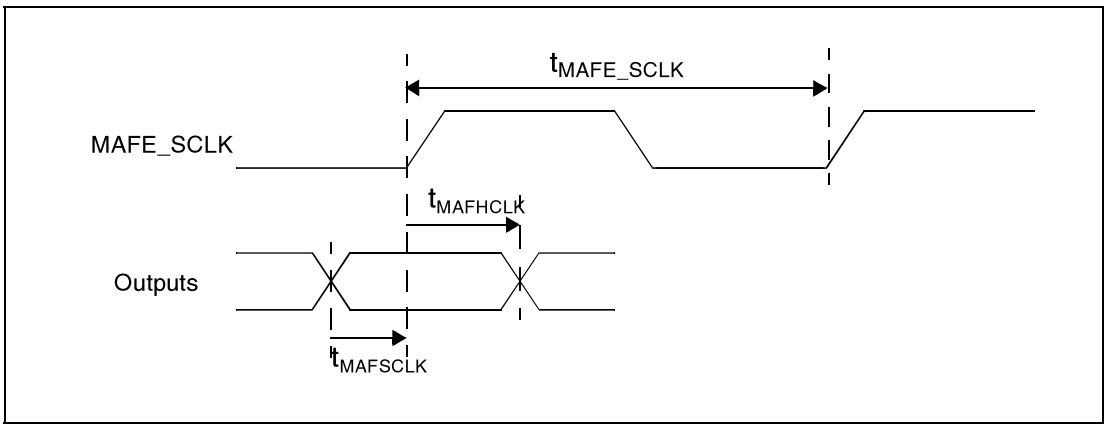


Table 62: MAFE interface input timings

Symbol	Parameter	Min	Max	Units
Input clock	MAFE_SCLK clock period		100	ns
$t_{MAFHCLK}$	Inputs setup to MAFE_CLK rising edge	20		ns
$t_{MAFSCLK}$	Inputs hold to MAFE_CLK rising edge	20		ns

12 HD and SD triple video DACs

12.1 Description

There are two identical sets of video DACs for HD and SD output. Both are triple high-performance 10-bit digital to analog converters, and consist of three 10-bit DAC modules joined together. The full-scale output for each DAC set is controlled by an external resistor.

Each DAC is able to drive 10 mA.

The blocks are powered by 2.5 V analog and 1.0 V digital supplies, with separate analog and digital grounds.

The blocks require a external precision resistor (R_{REF}) to provide a bandgap reference. The optimum R_{REF} value is 7.72 kΩ +/- 1%.

The blocks' analog current sources provide an voltage output range of 1.4 V, with an optimum linearity through an external precision resistor (R_{LOAD}). The R_{LOAD} optimum value is 140 Ω +/- 1%.

The exact calculation for the voltage output range is:

$V_{OUT} = 77.31 * (R_{LOAD}/R_{REF})$

with:

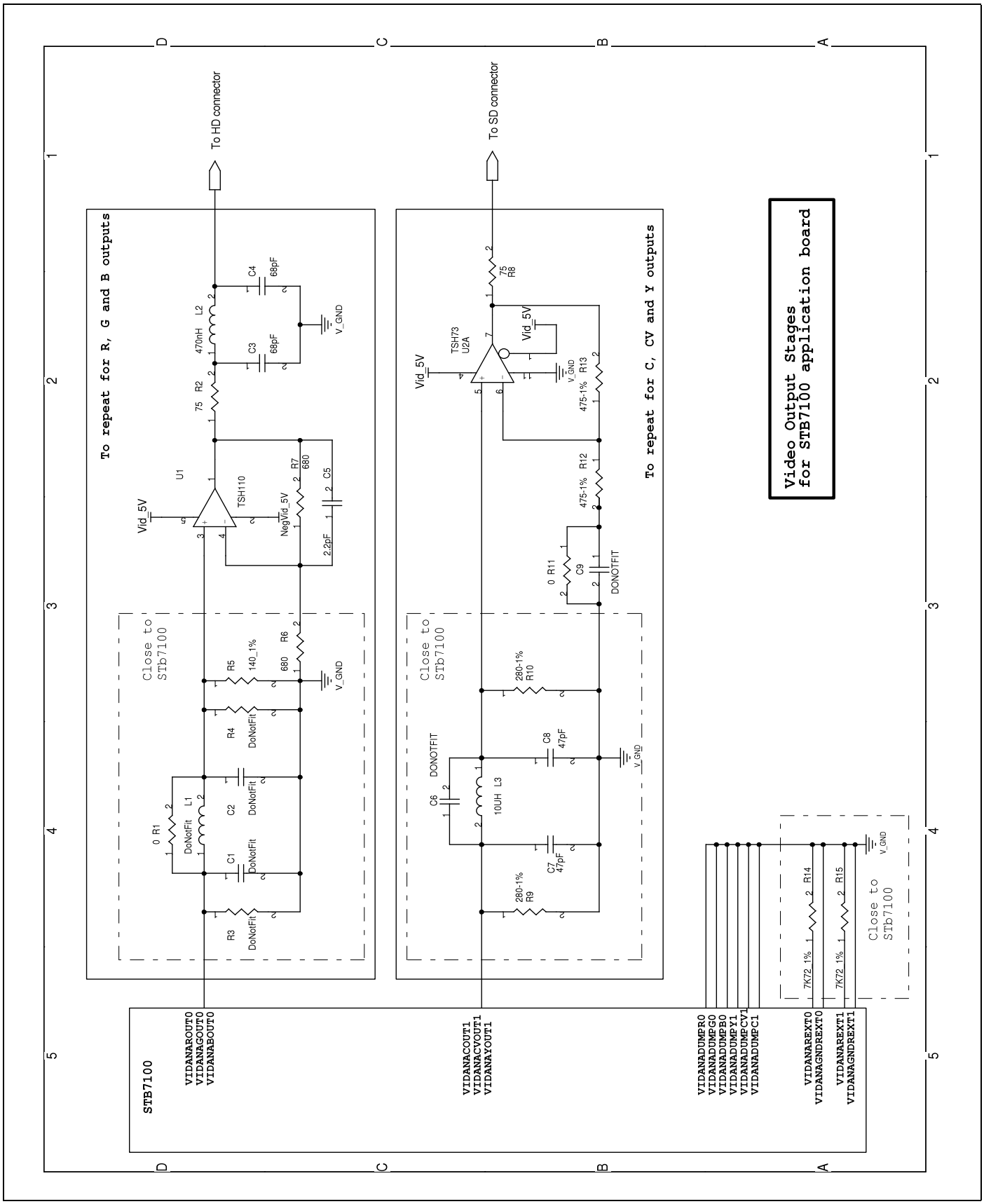
R_{REF} = reference resistor; maximum value is 7.72 kΩ

R_{LOAD} = load resistor

12.2 Output-stage adaptation and amplification

An example recommended video output stage with the external connections is shown in Figure 33.

Figure 33: Output stage schematic



13 Audio DAC

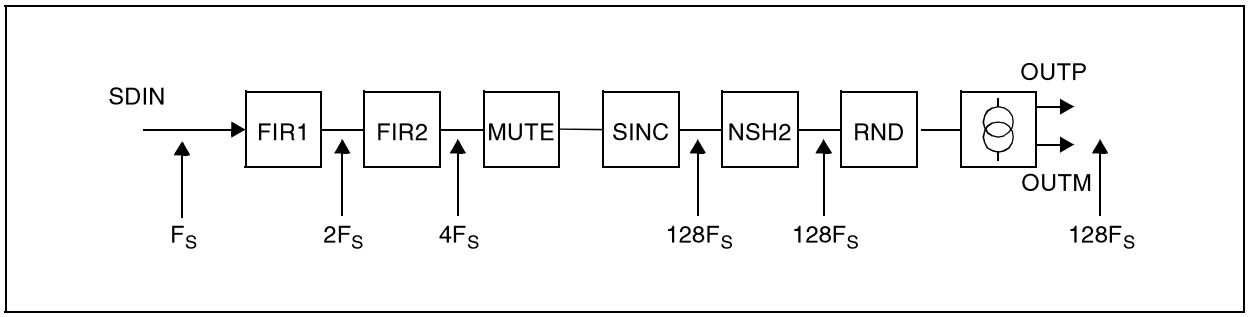
13.1 Description

The audio digital-to-analog converter (DAC) is a high performance stereo audio converter which accepts a 24-bit serial data stream from the audio decoder and converts it into a current source analog output signal. This signal is then filtered and transformed into a voltage output signal by an external analog filter.

The data converter uses a sigma-delta architecture which includes a second order noise shaper. The sigma delta modulator is followed by a 5-bit DAC to achieve at least 18-bit resolution.

This DAC can operate at sampling frequencies of 32, 44.1 and 48 kHz, or indeed any audio frequency up to 48 kHz.

Figure 34: Digital flow



The input stream SDIN derived from the audio decoder, sampled at F_S, is first interpolated by two and then filtered by a 75th order FIR filter, FIR1. This signal, at $2F_S$, is interpolated by two and filtered by a 20th order FIR filter, FIR2. The signal, at 4 F_S, can be soft muted by the MUTE block, and enters the SINC filter which interpolates by 32. The noise shaper then transforms this signal to five bits. A randomizer then expands the data to a thermometer code and permutes the sources to avoid mismatch between the 32 current sources.

The audio frequency synthesizer, within the clock generator, provides a system clock at 256 x F_S which is divided down internally to produce all other clocks.

The audio DAC group delay is 23 periods of the sampling frequency.

13.2 Operating modes

13.2.1 Reset

The audio DAC is reset by the chip global reset. The audio DAC can also be reset via the configuration register bit ADAC_CFG.NRST.

At reset, the audio DAC is disabled.

13.2.2 Power supplies

For better noise immunity, and to fulfill the specifications in terms of output range, the audio DAC has several different supply pairs.

- AUD_GNDA, AUD_GNDAS, AUD_VDDA: ground and 2.5 V analog supplies for the switches (control of the current sources) are supplied to the chip externally.
- GNDE_AUD_ANA, VDDE2V5_AUD_ANA: ground and 2.5 V analog supplies for the audio DAC pads ring are supplied to the chip externally.

13.2.3 Input/output signals

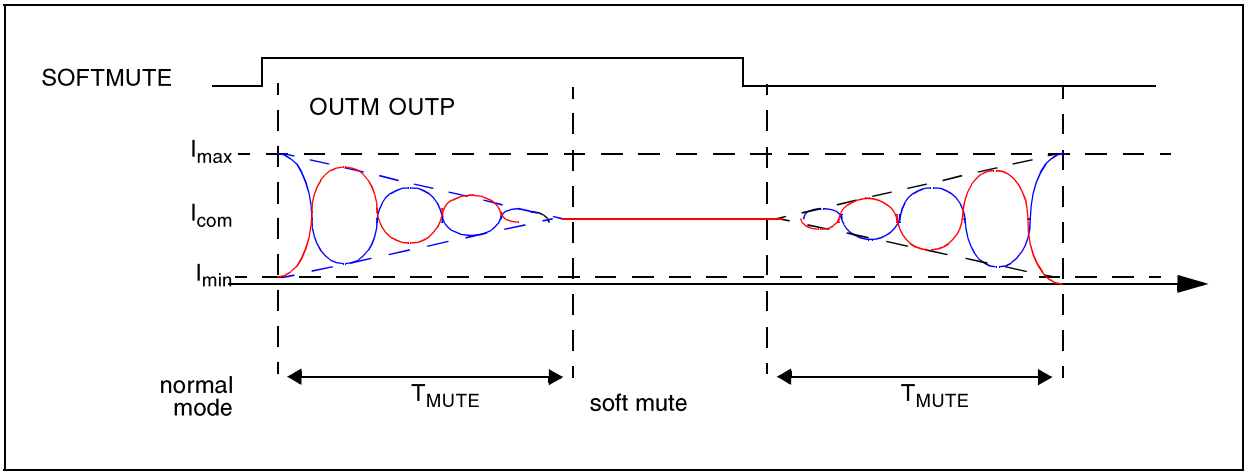
Table 63: Audio DAC output signals

Pin name	Description
AUDANAPRIGHTOUT	Right channel, differential positive analog output. The signal is then filtered.
AUDANAMRIGHTOUT	Right channel, differential negative analog output. The signal is then filtered.
AUDANAPLEFTOUT	Left channel, differential positive analog output. The signal is then filtered.
AUDANAMRIGHTOUT	Left channel, differential negative analog output. The signal is then filtered.
AUDANAIREF	DAC reference current output. This pin should be connected to an external resistor. 575 ohm +/- 1%.
AUDANAVBGFIL	DAC filtered reference voltage input. This pin should be connected to an external 10 µF capacitor (ground connection AUD_GNDA).

13.2.4 Soft mute

The mute function is controlled by bit ADAC_CFG.SMUTE. The current output signal (AUDANAPLEFTOUT/AUDANAPRIGHTOUT, AUDANAMLEFTOUT/AUDANAMRIGHTOUT) is first attenuated to 96 dB. When the output current reaches the common mode current I_{com}, the current sources are switched off one after the other in order to decrease the output current on AUDANAPLEFTOUT/AUDANAPRIGHTOUT. Once this sequence is complete, the analog part can be powered down. The total time for the mute/unmute sequence is at least 1920 sampling periods.

Figure 35: Soft mute and digital power down



13.2.5 Digital and analog power down

The digital part of the audio DAC can be disabled by setting ADAC_CFG.NSB to 0. An automatic soft mute avoids any pop noise.

The analog part of the audio DAC can be disabled by setting ADAC_CFG.PDN to 0. Depending on the external circuitry, pop noise may be unavoidable.

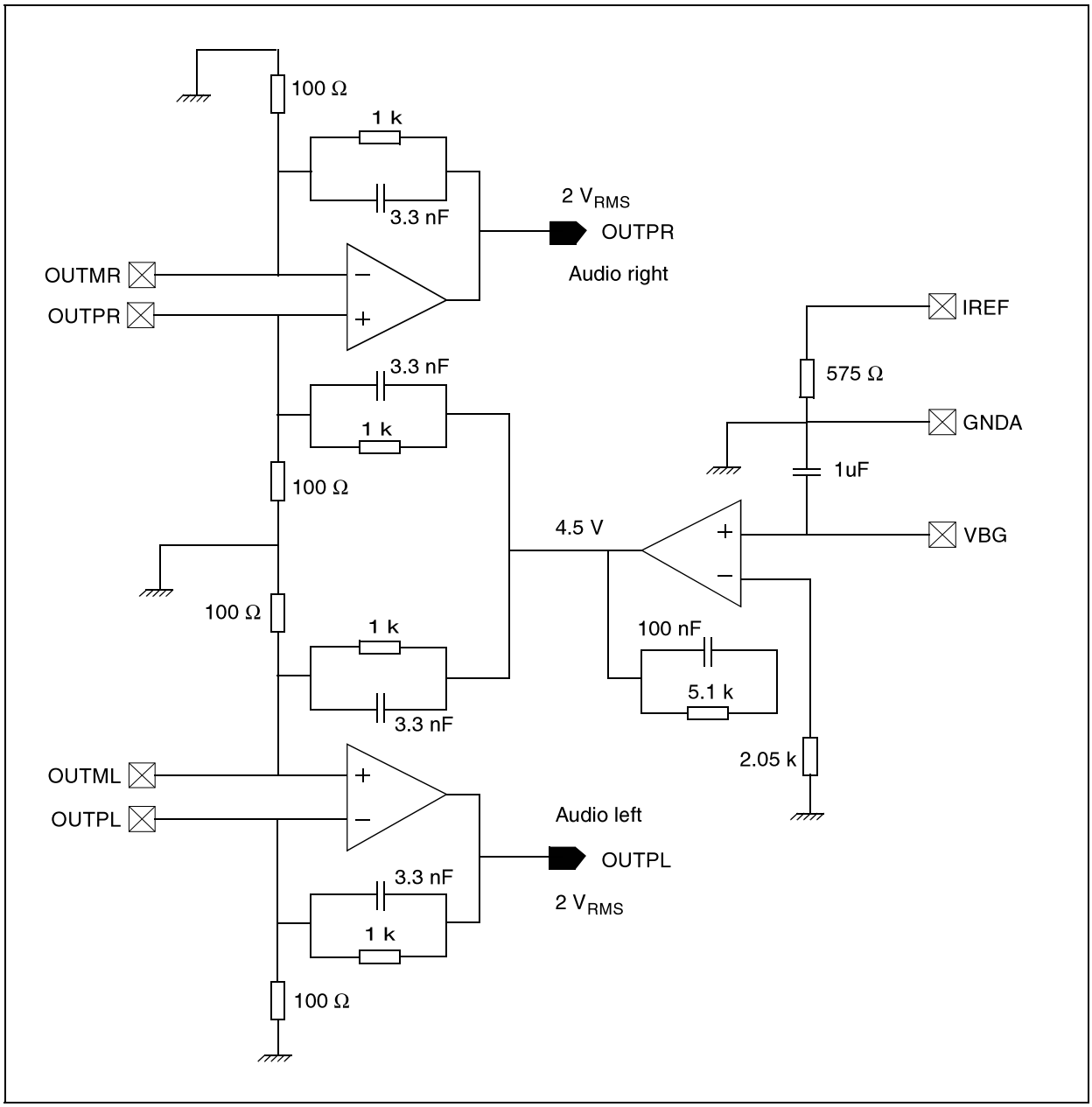
13.3 Output stage filtering

The audio DAC provides differential current source outputs for each channel. The use of a differential mode interface circuit is recommended to achieve the best signal to noise ratio performance. A single-ended mode interface circuit can be used, by grounding pins AUDANAMLEFTOUT and AUDANAMRIGHTOUT, but this is not recommended as the resulting signal to noise ratio is less than 90 dB.

An external 1% resistor R_{REF} should be connected to pin AUDANAIREF of the DAC. A typical value for R_{REF} is 575 Ω to get proper band gap functionality.

Figure 36 shows an audio output stage to deliver a 2 V_{RMS} signal.

Figure 36: 2 V_{RMS} schematic with +9 V power supply



14 PCB layout recommendations

14.1 SATA

To meet SATA specifications, some rules must be followed when designing the PCB.

Recommendations include power supply quality requirements and routing requirements for signal integrity.

14.1.1 Power supplies

To operate correctly, the SATA PHY must be isolated from the surrounding noise. This can be achieved by using a clean voltage source (linear DC regulator) and/or passive high-frequency filtering.

14.1.2 Voltage regulator

A dedicated voltage regulator for the SATA PHY is recommended.

The voltage regulator must be linear or LDO (switching or DC/DC regulators cannot be used).

A regulator with 2% spread around the nominal voltage is recommended.

The power supplies SATAVDDDLL, TMDSVDDX, LMISYSDLL_VDD, and LMIVIDDLL_VDD must be carefully designed since they are used for the high frequency clock generation.

The MDLL does not tolerate more than 50 mV of noise, specially below 10 MHz.

14.1.3 Power supplies passive filtering

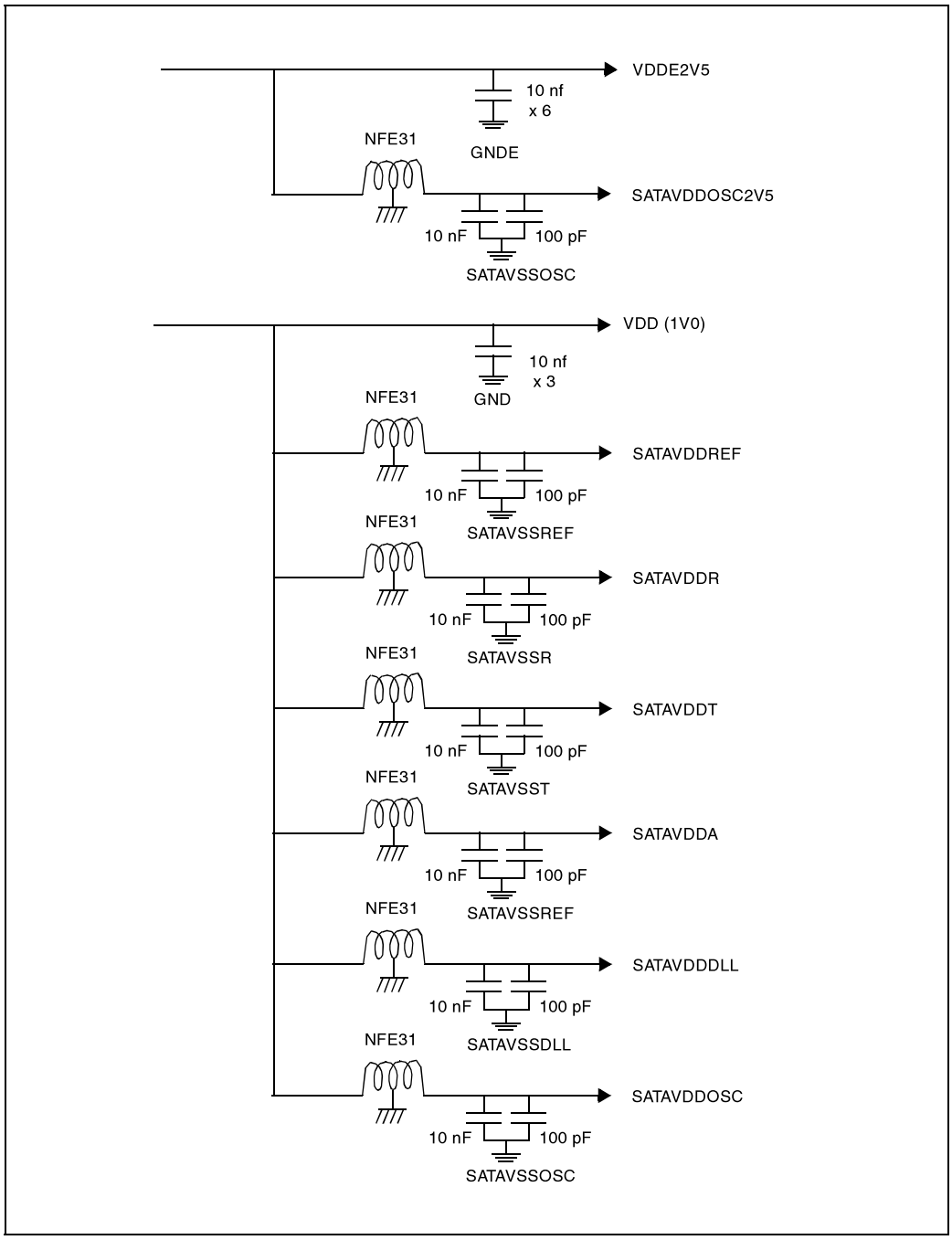
To achieve the necessary isolation from power supply noise, passive filter networks are required. This passive filtering avoids interference to the PHY from other sources, including the different power sources of the SATA. The most noisy source is VDDT.

14.1.4 Reference crystal

One possible quartz crystal to use is the EPSON FA-365, 30 MHz.

14.1.5 SATA interface filtering

Figure 37: SATA interface filtering



14.1.6 High speed serial trace routing

The PCB routing must be done with the following guidelines.

14.1.6.1 Ground plane

Microstrip with ground reference plane implementation is preferred.

No other signal than SATA should overlay the reference plane.

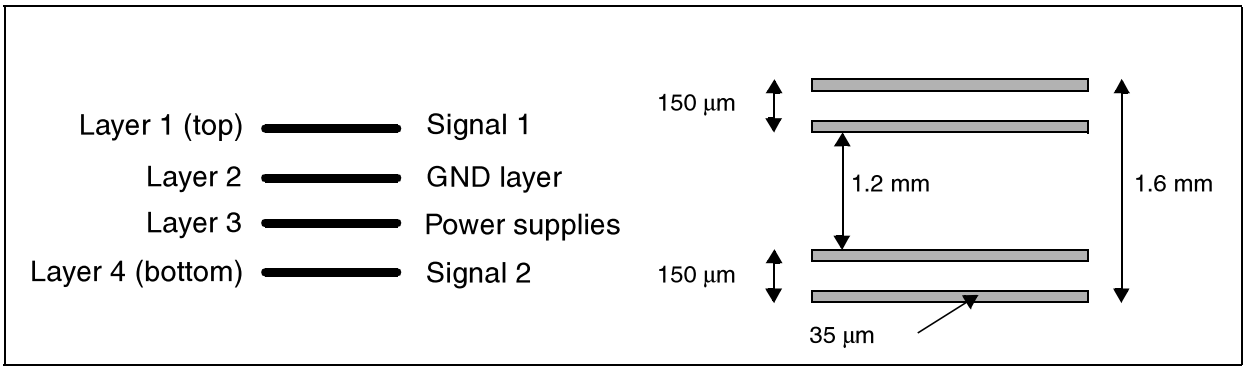
14.1.6.2 Differential signal pair routing

TXP/TXN and RXP/RXN are differential signals as defined by SATA spec.

- The distance from the chip to the SATA connector must be as short as possible.
- When routing a differential pair, the complementary signals must be matched in length. (<0.5 mm)
- No right angle allowed
- If a signal has to change layers, attention must be paid when adding a via about the return current: use a stretching ground via.
- Both traces of a differential pair must have a 50 Ω impedance to ground, without any impedance discontinuity from the chip to the SATA connector. This actually makes a differential impedance of 100 Ω and a common mode impedance of 25 Ω
- Vias act as strong impedance discontinuities: avoid them in the differential traces.
- Signal routing are preferred at top level.

Figure 38 below describes a PCB stack, with differential signals. The differential pair is preferably routed on the top layer. It is also possible but less recommended to route the differential signals on the bottom layer.

Figure 38: PCB stack with differential signals



The two traces of a differential pair must be loosely coupled, that is, their impedance to ground must be controlled and equals to 50 Ω The traces must be far enough from each other to ensure a low direct coupling between themselves.

14.1.6.3 AC coupling

The SATA PHY works in AC coupled configuration.

The AC capacitance has to be put on RX on the connector side (capacitance value = 10 nF, 12 nF max in the SATA specification).

14.2 DDR-SDRAM interface

14.2.1 Recommended PCB

To ensure better signals integrity and also to comply with the high density of the BGA package, it is recommended to use a 4-layer PCB with the following stack:

- Layer 1: Signal 1,
- Layer 2: Power plane,
- Layer 3: Ground plane,
- Layer 4: Signal 2.

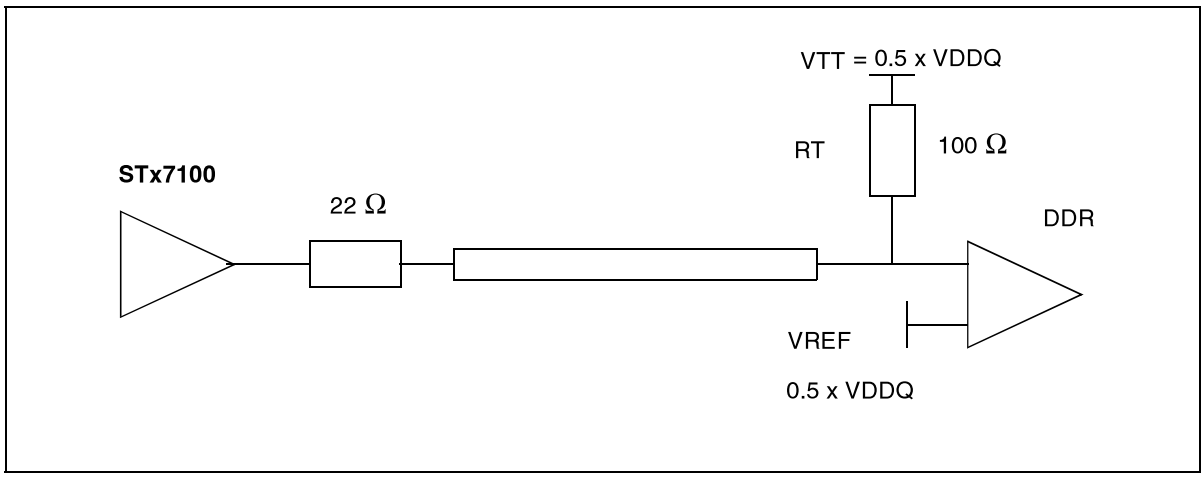
14.2.2 System considerations

To achieve a high bandwidth on the local memory interface, the STx7100 incorporates SSTL_2 buffers. At the board level it is therefore recommended to follow SSTL-2 signalling design rules.

The use of this high speed logic requires series resistors, parallel termination schemes and reference voltage circuitry.

The most suitable scheme is shown below. This reduces reflections, improves signal bandwidth and settling.

Figure 39: SSTL_2 Single terminated line



14.2.3 Power supply recommendations

An important point to take into consideration when designing such systems is to guarantee that both the STx7100 and the DDR devices have very clean digital power supplies.

To decouple the STx7100 requires more decoupling capacitors. To better achieve a good power supply decoupling, it is recommended to equally distribute 100 nF ceramic capacitors and 1 µF Tantalum capacitors over the LMI power supply pins.

14.2.4 Reference voltage

Both the STx7100 and the DDR devices require a reference voltage, so called VREF in Figure 39.

Some attention should be paid to the routing of VREF, since the SSTL_2 specification requires dynamic noise to be maintained to less than 2% of the VREF DC level.

It is recommended to decouple VREF to both VDDQ and VSSQ with balanced decoupling capacitors. The use of 100 nF ceramic capacitors is adequate to do so. A decoupling capacitor pair is recommended at each device location (DDR + STx7100).

It is necessary to keep VREF isolated from induced noise as possible. VREF should be routed over a reference plane, and preferably shielded. Layer 2 is preferable.

14.2.5 Termination voltage

The VTT generation circuit should be placed as close as possible to the parallel termination resistors to reduce the impedance and length of the signal return path.

The termination voltage should be routed to all the termination resistors through a thick copper track, with a minimum width of 1500 mils.

The termination resistors should be placed as close as possible to the DDR memory. Use of 5% resistors is adequate.

Resistor packs are acceptable, but signals within an RPACK must be from the same DDR signal group. No mixing of signals from different DDR signal groups is allowed within an RPACK. The parallel termination resistors connect directly to the VTT track with the shortest wire as possible.

VTT requires some decoupling capacitors close to RPACK. VTT should be routed over a reference plane.

On a 4-layer PCB, the most appropriate layer to route the termination voltage track is the layer 2 as it will not interfere with the signals routing that is the most critical part.

14.2.6 Memory bus layout general considerations

The memory interface bus can be split in three groups:

- the data bus and its associated strobes DQM and DQS,
- the address bus and associated control signals RAS, CAS and Write,
- the differential clock signals.

Each group requires specific attention described in details in the next paragraphs, but some general layout rules apply:

- Maintain the ground layer as a reference plane for all memory signals, that is, do not allow splits in the plane underneath both memory and STx7100 LMI.
- Series resistors should be placed as near to the close to the driver pin as possible. For the data bus, resistors should be placed at mid point because of bidirect transmission.
- As much as possible all signals should be routed without any via between the STx7100 and the memories. In all cases, minimize the usage of vias.
- All DDR traces should be as short as possible (not longer than 3 inches), and traces within a group should have close length in order to reduce the skew between different lines.
- All signal traces except clocks are routed using 5/5 rules. (5 mils traces and 5 mils minimum spacing between adjacent traces).
- Clocks are routed using 5 mils traces and 5 mils space to the 5 mils ground trace.

14.2.7 Address bus and control signals layout

For the address bus and the control signals, a branch type net topology is recommended for better signal integrity and smaller skew than daisy chain type.

14.2.8 Data bus layout

- Data lines and strobe signals within each byte group (for instance DQ[0 .. 7] and DQS0 and DQM0) should be routed so that the maximum difference in their lengths is minimum.
- Bit swapping within a byte group is permitted to facilitate routing.
- The DDR_DQS signal should have a length that is close to the longest other trace within its byte group.

14.2.9 Clock signals layout

- Minimize the usage of vias as much as possible.
- Clocks should have a 5 mill ground trace surrounding them, with vias stitched to ground at 0.5 inch intervals, or as often as routing allows.
- The CLK and N_CLK signals must be routed as differential signals in order to have a correct crossing point, that is, with identical lengths. This differential pair should be terminated by a 100 Ω resistor connected between both signals, and placed close to the memory chips.

14.3 USB2.0

14.4 Board design

Each guideline in this section (1, 2, 3…) has a reference attached to it indicating it is a board guideline.

14.4.1 Layer stacking

Guidelines provided in this document refer to a four-layer PCB stack up. In one case a two-layer PCB stackup is also shown. Board stackup can be done in two ways, as shown below. In either way, DPDN should be referenced with respect to the ground plane as shown. For an *n*-layer board (where $n > 4$), always reference the DPDN signals with respect to a ground plane.

1. DPDN on the top layer.

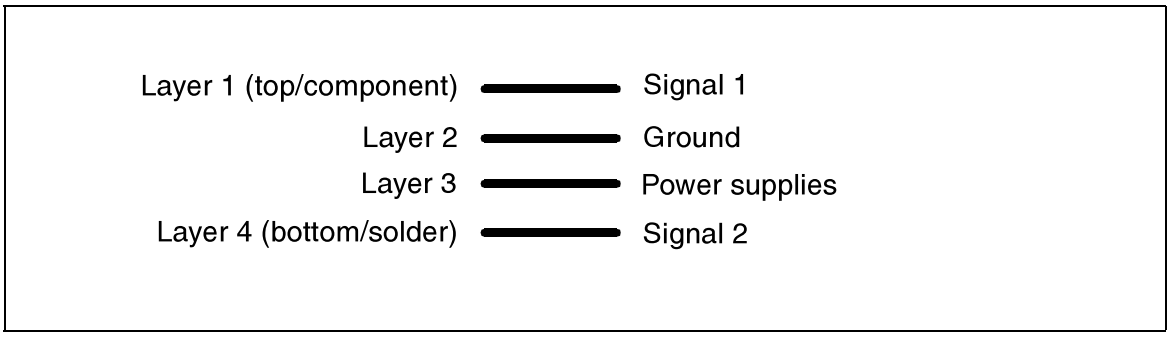


Figure 40: PCB Layer stackup - DPDN on top layer

2. DPDN on bottom layer:

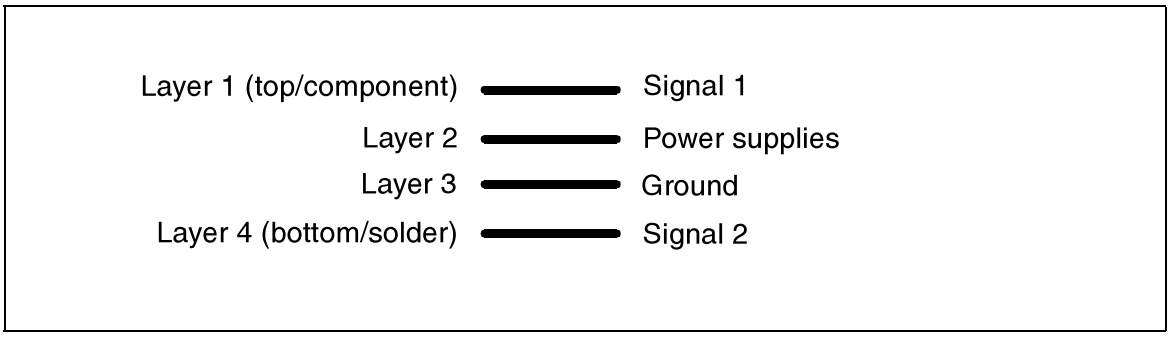


Figure 41: PCB Layer stackup - DPDN on bottom layer

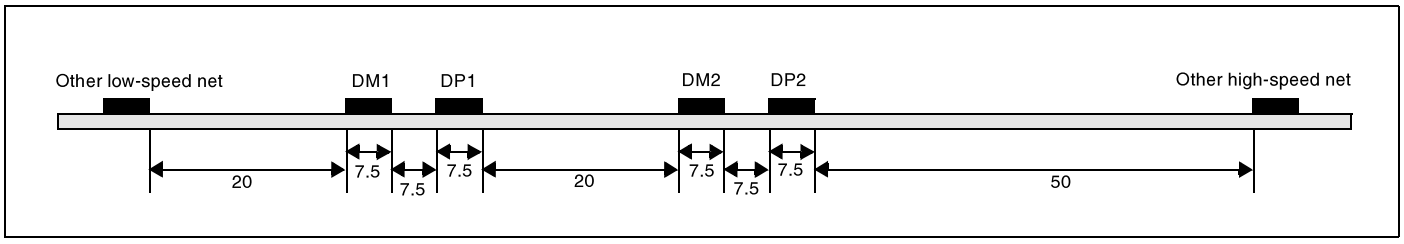


Figure 42: Recommended trace spacings (mils) for the above stackups

3. Follow Figure 42 for spacing other high- and low-speed nets; see rules 17 and 18. This diagram shows the trace geometry for a four-layer PCB. It can change with the number of layers present in the PCB.

14.4.2 Layout suggestion for the crystal

4. Avoid running traces below the crystal.
5. If surface mount crystal is used, place load capacitors on same side as surface mount crystal.
6. Do not route the traces between the crystal pins and the load capacitors through vias.
7. Load capacitors need to be located next to crystal pins.
8. Figure below shows how to do layout for the crystal. Both traces on left and right should be equidistant. A 30 MHz crystal can be chosen.
9. For the value of load cap, refer to the datasheet of crystal manufacturer. It should be a value below 33 pF.

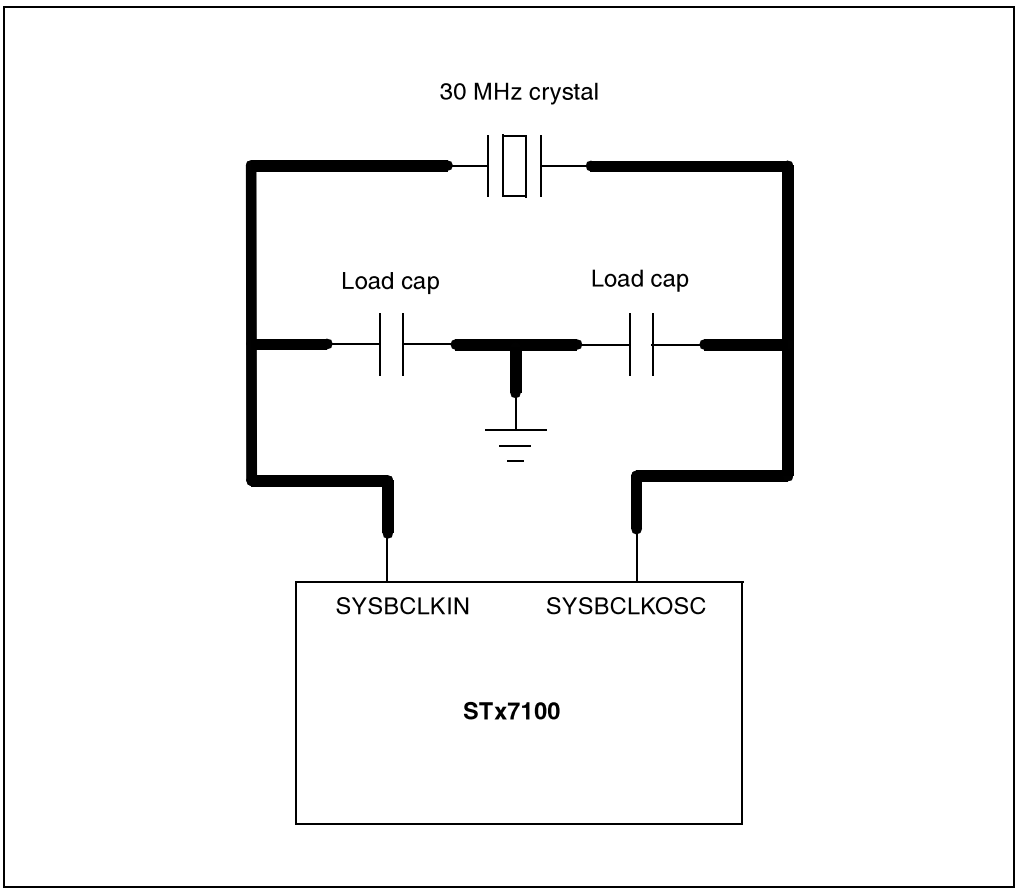


Figure 43: Recommended layout for crystal

14.4.3 USB connector

10. Pin 4 of the USB receptacle “GND” should be connected to the signal ground.
11. Chassis of the receptacle should be connected to pin 4 of USB receptacle.

14.4.4 Chassis and signal grounds

12. The chassis should be connected to the signal ground through an inductor/capacitor/ resistor.

14.4.5 DP and DN signals

13. For a 4-layer PCB, 7.5-mil traces with 7.5-mil spacing results in approximately 90 Ω differential trace impedance for DP and DN. For height above ground plane refer to rule 32. This point should be double checked by the PCB layout designer using an impedance calculator.
14. For a 2 layer PCB, Refer to rule B-31.
15. For an *n*-layer PCB where $n > 4$, rules 30 and 31 may not be applicable. Hence use an impedance calculator to get the trace geometry.
16. Use 20-mil minimum spacing between high-speed USB signal pairs (DPDN) and other low speed non periodic signal traces for optimal signal quality. This helps prevent crosstalk.
17. Use 50-mil minimum spacing between high-speed USB signal pairs (DPDN) and clock/high speed/periodic signals.
18. Differential impedance should be strictly respected: 90 Ω diff.
19. Routing should be with minimum vias (avoid if possible), no right angle, only 45 degrees (or round corners) turn with smooth edges.
20. Length of DPDN, traces should be kept at a minimum as possible.
21. High-speed USB signal pair traces should be trace-length matched. Max trace-length mismatch between High-speed USB signal pairs (such as DN and DP) should be no greater than 150 mils.
22. Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
23. Do not place any zero Ω resistors on DPDN lines as this would change characteristic impedance.
24. Routing of DPDN lines should be avoided within 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

14.4.6 REF connection

25. An external reference resistor R_{REF} should be connected to the ground of compensation block VSSC2V5 and its value should be 1.5 KΩ ±1%.
26. Note do not choose 10% tolerance resistors.

14.4.7 Other

27. External components quartz (24 or 30 MHz), 1.5 KΩ±1%, filters, decoupling capacitors needed.
28. No other external components required (like suppressor capacitors of 50 µF) for ESD protection of data lines. DN, DP pads have built in ESD protection.
29. Do not place any common mode chokes for controlling EMI. This would degrade the signal quality and cause eye diagrams to fail.

14.4.8 View of a PCB impedance calculator

The Following screenshots clearly define the trace parameters for 2- and 4-layer PCBs.

30. Two-layer PCB:

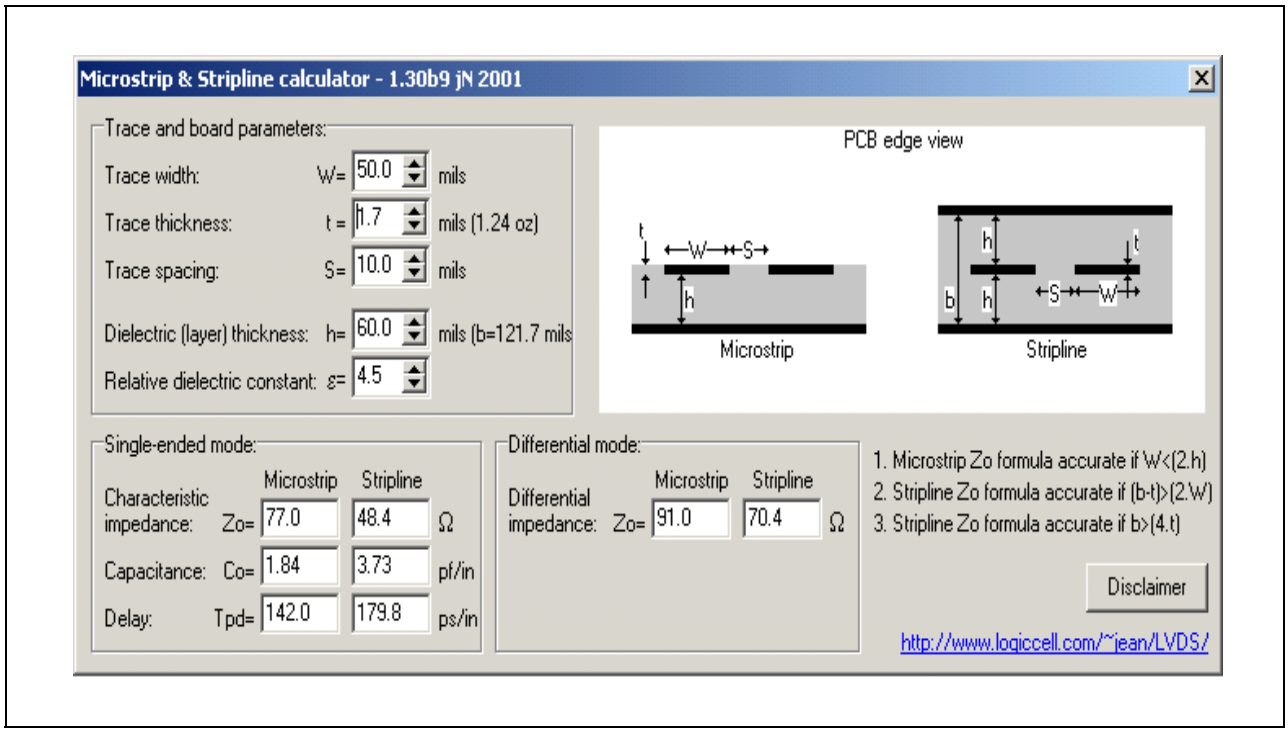


Figure 44: Trace geometry for two-layer PCB

31. Four-layer PCB:

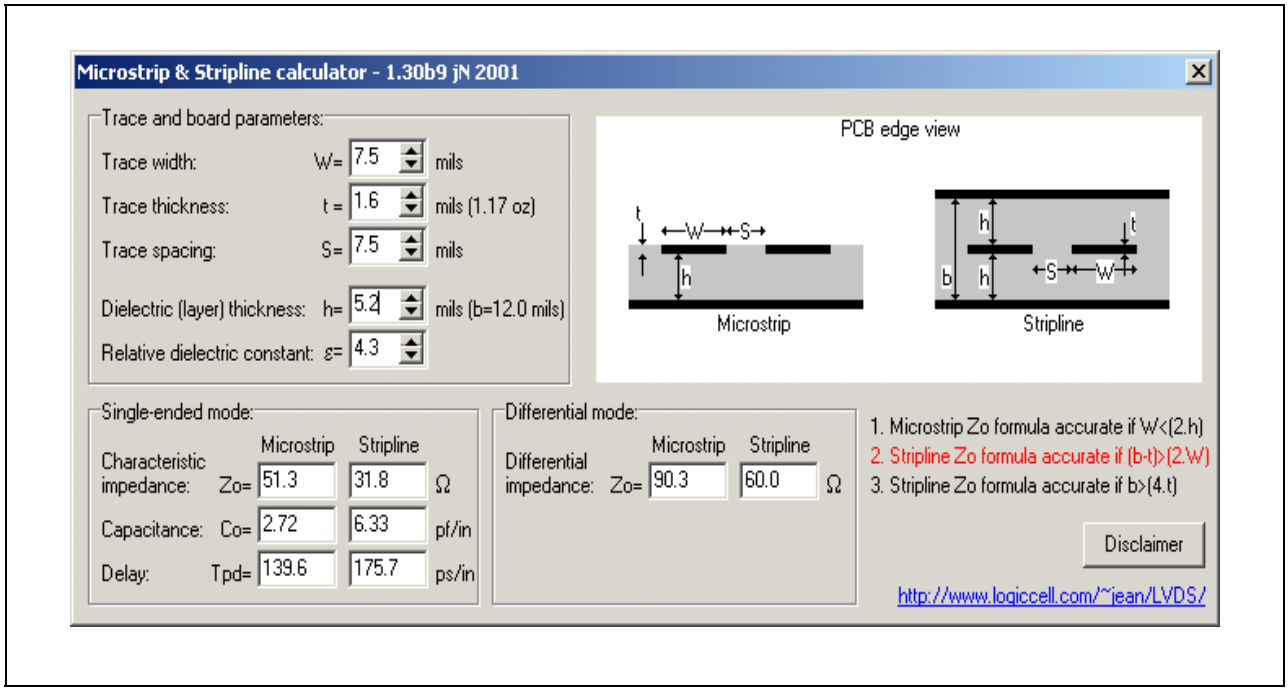


Figure 45: Trace geometry for four-layer PCB

14.5 Power supplies

14.5.1 Power supplies required by the Phy IP

Symbol	Description	HC (Volts)
USBVDDP2V5	USB2 2.5V PLL power	2.5
USBVDDP	USB2 PLL power	1.0
USBVDDB3V3	USB1.1 mode buffer power	3.3
USBVDDBC2V5	USB2 2.5V buffer power	2.5
USBVDDBS	USB2 buffer/serdes power	1.0

Table 64: Description of supply voltages

14.5.2 Recommended filters

32. The Phy IP needs > 3 dB attenuation of all frequencies above 1.2 MHz.
The attenuated noise ripple at VDDBS should be < *x* mV (pk-pk), where:
x = 20 for *f* (ripple frequency in MHz) >= 1.2
x = 20/(sin((pi**f*)/1.2)) for *f* (ripple frequency in MHz) < 1.2
Similarly, for other supply/ground, the attenuated noise ripple should be < *y* mV (pk-pk), where:
y = 50 for f (ripple frequency in MHz) >= 1
x = 50/sin(pi**f*) for *f* (ripple frequency in MHz) < 1
According to this, a suitable filter has to be chosen.
Ferrite inductor 2200 pF Type NFM60R, 25 V, 6 A component from Murata must be used.

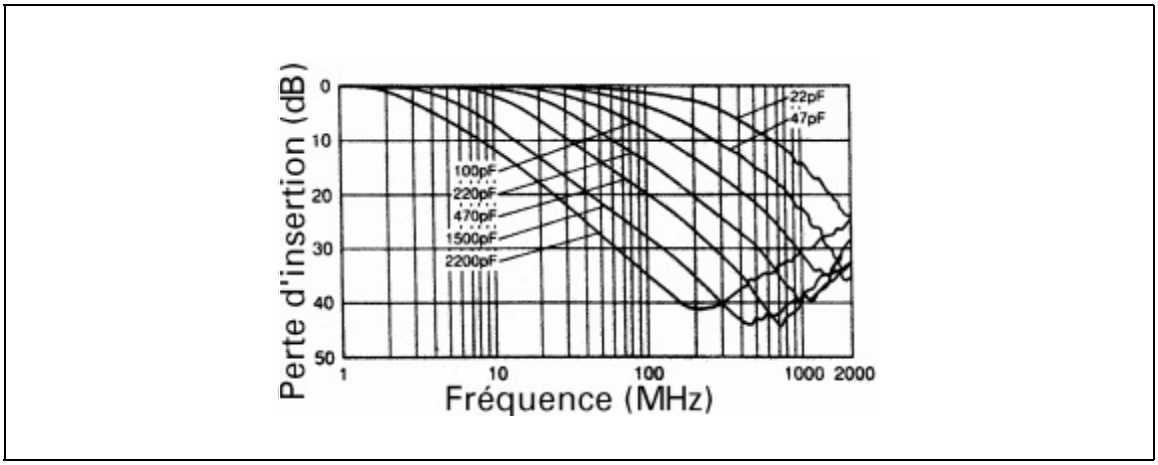


Figure 46: Recommended filter response

14.5.3 Sharing of supplies

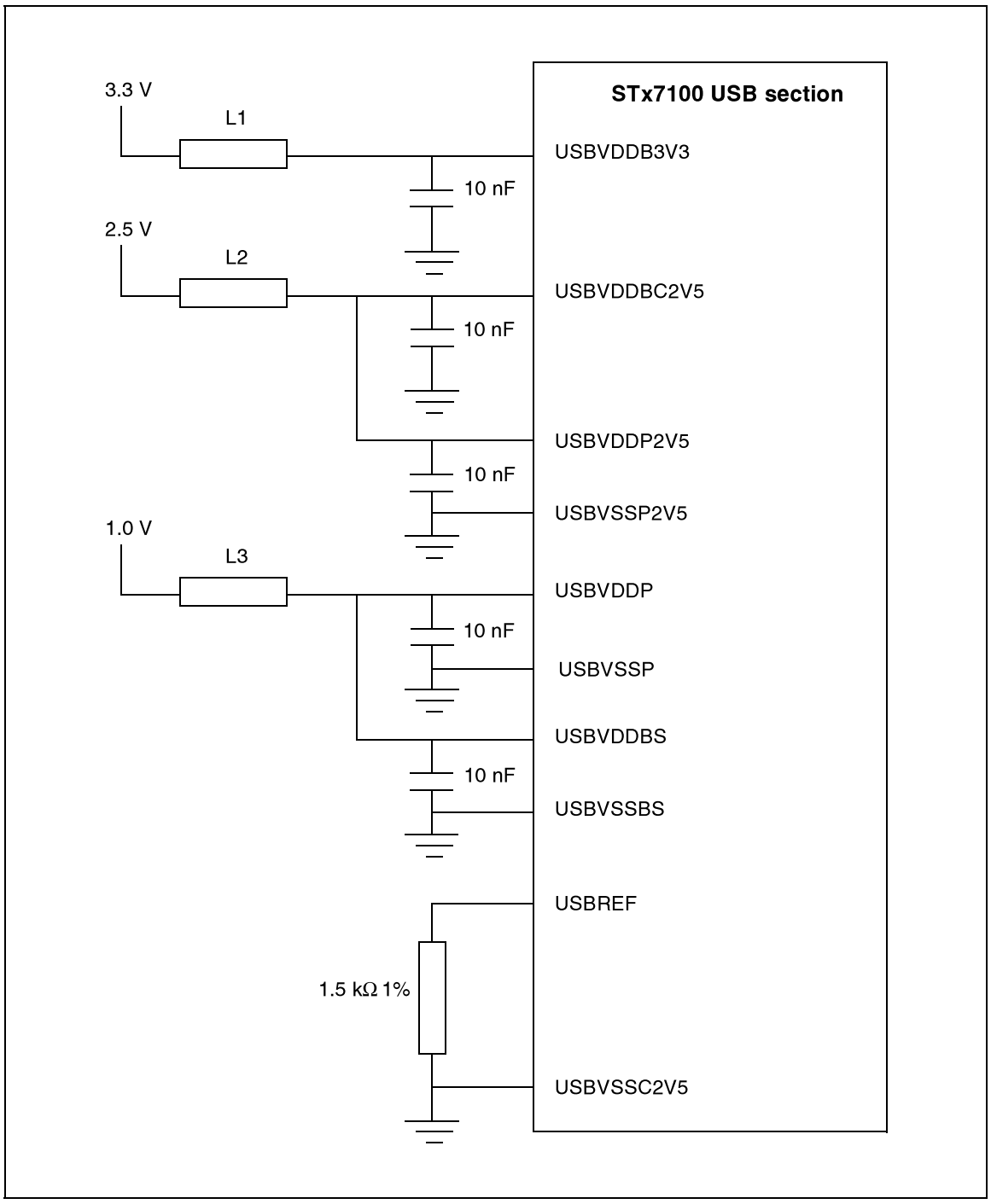
33. Connection of USB analog supplies with other digital supplies should be avoided. This creates a dependency of digital activity of the SOC and DP/DN quality.

14.5.4 Power distribution scheme and on-board filtering of individual power supplies

Filters and decoupling capacitors must be used to limit the noise environment for each and every power supply. Place all decoupling capacitors very close to the balls. R_{REF} should also be placed as close as possible to the ball of ASIC and connected to USBVSSC2V5.

34. The grounds of the decoupling capacitors are connected to their respective VSS. A value of 10 nF is recommended for decoupling capacitors.

Figure 47: Example filtering scheme



14.6 HDMI

When designing the HDMI interface, the signal traces should have the same length and must be kept as much as possible on the same layer. No additional external components are required.

Part 3

System infrastructure

15 Clocks

15.1 Overview

The STx7100 includes three clock generator (clockgen) subsystems:

- **Clock generator A** generates clocks for the CPUs, memories and STBus. It comprises two PLLs (PLL0 and PLL1) and programmable dividers to generate the group A clocks.
- **Clock generator B** generates clocks for the video, displays, transport and peripherals. It comprises two frequency synthesizers banks (FS0 and FS1), programmable dividers and a clock recovery module.
- **Clock generator C** generates the audio clocks. It comprises three independent audio frequency synthesizers (described in Chapter 59: *Audio subsystem* *on page 731*).

Clock input/output pins

The group A clocks take a reference input clock from the SYSACLKIN pin. This is a single input requiring an external oscillator. The default values of group A clock generation parameters are based on a 27 MHz reference clock. This is the recommended reference clock frequency; however, other clock values less than 40 MHz may be used.

The SYSBCLKIN/SYSCLKOSC pair is a crystal interface which is part of the SATA analog interface which integrates an oscillator requiring a 30 MHz crystal. In addition to driving the SATA and USB interface, this clock can be used as a reference clock to generate the group B and group C clocks.

The SYSBCLKINALT input provides an alternate reference clock for the group B and group C clocks instead of using the oscillator clock inside the SATA Phy. The default state is to use the 30 MHz SATA clock, but the alternate reference clock can be selected via registers CKGB_REF_CLK_SEL and AUD_FSYN_CFG. This input pin can be connected to the same reference clock that is input on the SYSACLKIN pin. The SYSBCLKINALT input can range from 27 MHz to 30 MHz. The programming of the frequency synthesizers must take into account the reference clock frequency.

The internal clocks can be observed or used as an auxiliary clock via the SYS_CLK_OUT pin, which gives access to the clocks of clockgen A. The clocks from clockgen B can be observed via an alternate PIO pad (PIO5 bit 2).

Encoder clock recovery

The STx7100 integrates a clock recovery module to recover the encoder clock. This module (DCXO) uses digitally controllable frequency synthesizers and an integrated digital clock recovery module. This feature can replace the external VCXO oscillator functionality and allows the use of a fixed oscillator. External VCXO functionality is still available in this mode however.

When an external VCXO is used, it must be connected to SYSBCLKINALT; SYSACLKIN can be connected to either a fixed oscillator or the VCXO.

When the DCXO is used, the SYSACLKIN pin is connected to a fixed oscillator and SYSBCLKINALT is either connected to SYSACLKIN or left unconnected (in this case, the SATA/USB 30 MHz clock is used).

Clockgen B includes a recovered 27 MHz clock. This clock is used for the programmable transport interface (PTI)'s system counter. The counter is used to compare arriving PCRs.

The alternative clocking schemes are summarized in Figure 48 and Figure 49.

Figure 48: STx7100 clocking scheme with an external VCXO

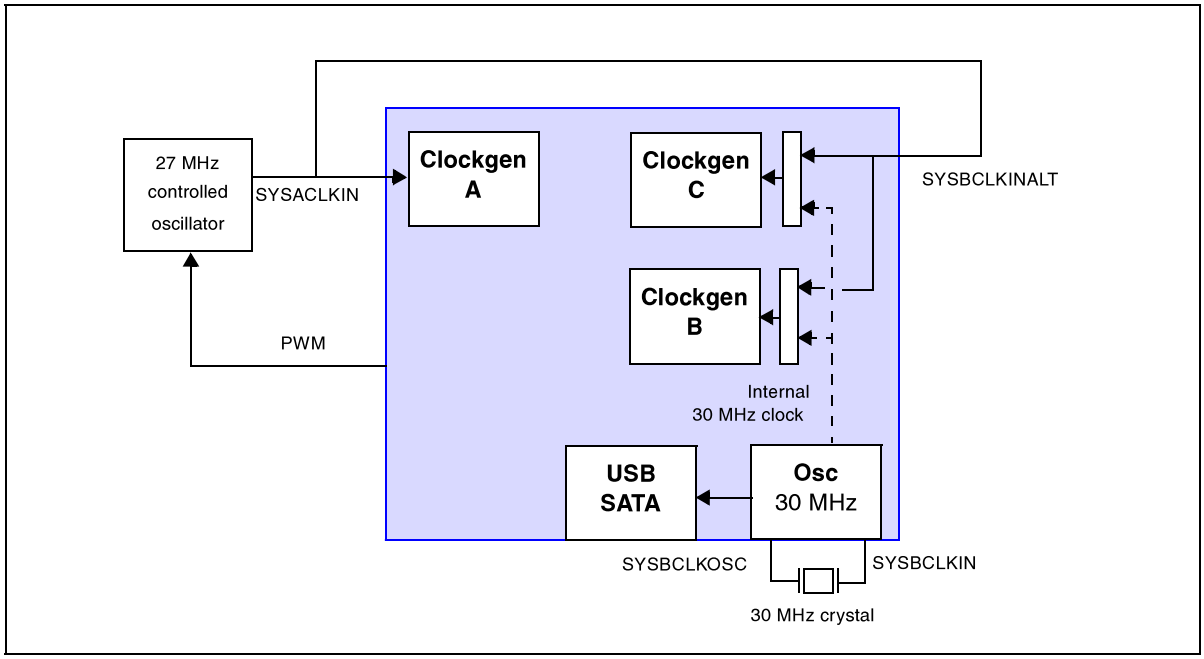
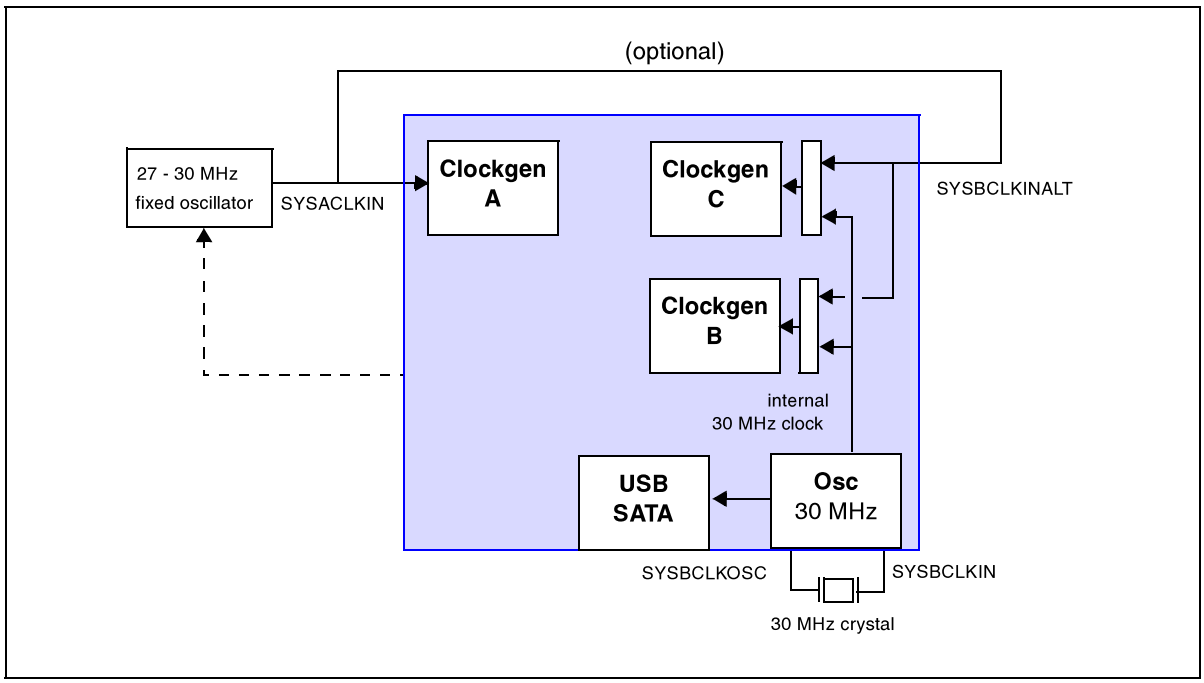


Figure 49: STx7100 clocking scheme with the internal DCXO



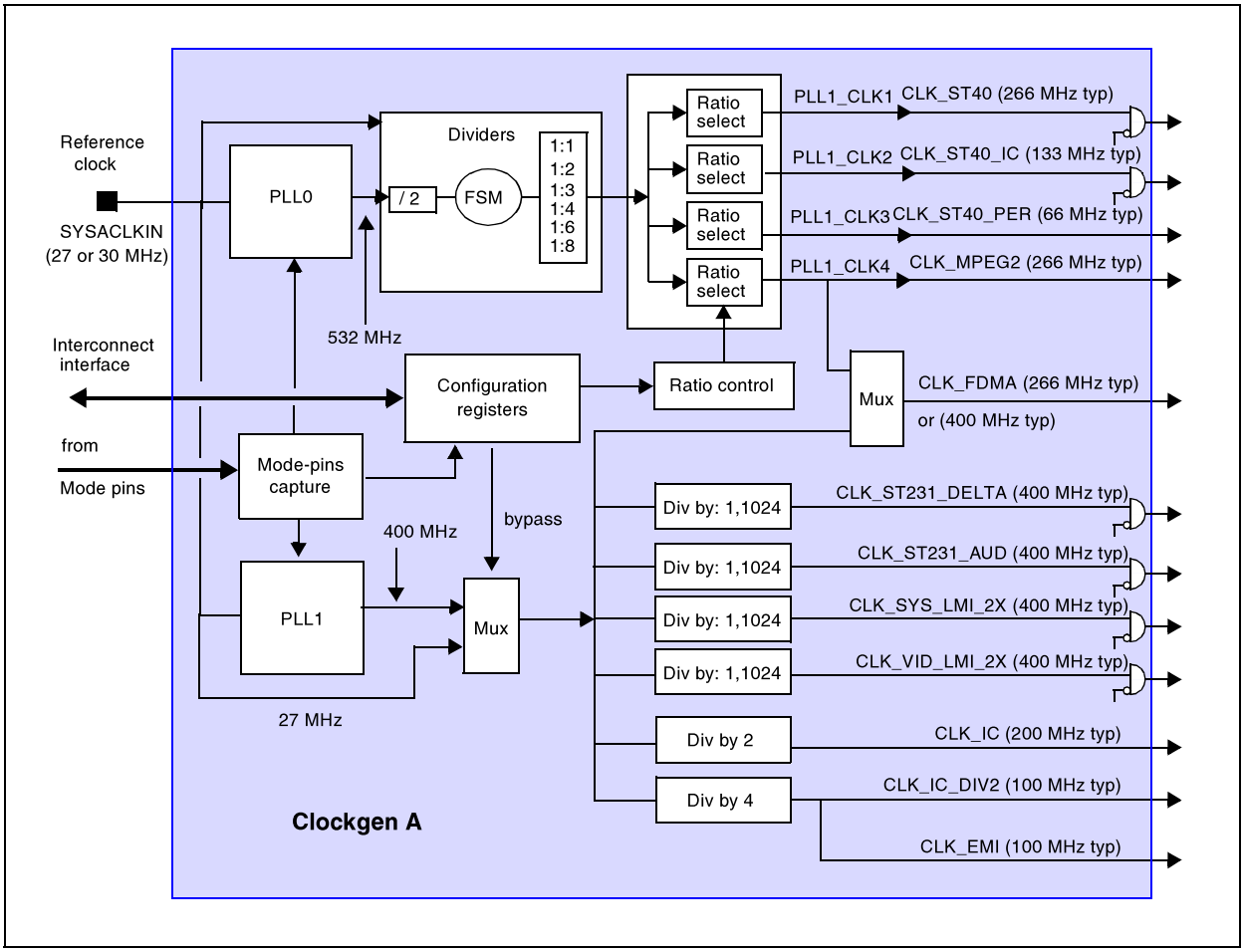
15.2 Clock generator A

Clockgen A includes two PLLs and produces the clocks for the CPUs, DDR interfaces, EMI interface, FDMA and interconnect.

The block diagram of this clockgen is shown in Figure 50.

15.2.1 Block diagram

Figure 50: Clockgen A block diagram



15.2.2 Clock signals

The group A clocks with their typical frequencies are described in Table 65.

The clock frequencies can be changed via clockgen A configuration registers.

Table 65: Clockgen A signals

Clock name	Typical frequency (MHz)	Description
CLK_ST40	266	ST40 core clock
CLK_ST40_IC	133	ST40 bus clock
CLK_ST40_PER	66	ST40 peripheral clock
CLK_FDMA	266	FDMA processing clock
CLK_MPEG2	266	MPEG2 decoder clock
CLK_SYS_LMI_2X	400	2x DDR clock for SYS LMI interface
CLK_VID_LMI_2X	400	2x DDR clock for VID LMI interface
CLK_ST231_AUD	400	Audio decoder ST231 core clock
CLK_ST231_DELTA	400	MPEG4 decoder ST231 core clock
CLK_IC	200	High-speed interconnect clock
CLK_IC_DIV2	100	Low-speed interconnect clock
CLK_EMI	100	EMI clock

15.2.3 Startup configuration

Clockgen A provides default configurations upon reset for its PLL0 and PLL1.

These configurations are defined by four external mode pins: EMIADDR[4:1] (see Chapter 9: *Reset configuration (mode pins)* on page 89)

The startup clock frequencies of clock generator A are shown below.

The recommended configuration is to use mode 0 for both PLL0 and PLL1.

Table 66: PLL0 startup configurations

PLL0 mode	EMI_ ADDR [2:1]	PLL0 state	MHz				
			PLL0 output	CLK_ST40	CLK_ST40_IC	CLK_ST40 _PER	CLK_FDMA
0	00	ON	532	266	133	66.5	266
1	01	ON	400	200	100	50	200
2	10	OFF	27	13.5	6.75	3.375	13.5
3	11	ON	600	300	150	75	300

Table 67: PLL1 startup configurations

PLL1 mode	EMI_ ADDR [4:3]	PLL1 state	MHz			
			PLL1 output	CLK_SYS/VID_LMI_2X CLK_ST231_AUD CLK_ST231_DELTA	CLK_IC	CLK_IC_DIV2 CLK_EMI
0	00	ON	400	400	200	100
1	01	ON	333	333	166	83
2	10	ON	266	266	133	66.5
3	11	OFF	27	27	13.5	6.75

15.2.4 Clock frequency change

The clockgen always starts with the configuration defined by the mode pins. Nevertheless, the clocks frequency can be changed with configuration registers. This initial configuration can be read in register MD_STA.

Clockgen programming lock/unlock

To prevent any unwanted clockgen reprogramming, the CGA_LCK register provides a protection mechanism. This register must be written first with the keyword “0xC0DE” to authorize any clockgen registers update. Writing any other value locks all clockgen A registers.

Clock ratio change without changing PLL0 and PLL1

The clock ratio can be changed on the fly without changing the PLL0 setup for the clocks CLK_ST40_IC, CLK_ST40, CLK_ST40_PER, CLK_FDMA and CLK_MPEG2. The clockgen design ensures a glitch-free frequency change.

The clocks CLK_SYS_LMI_2X, CLK_VID_LMI_2X, CLK_ST231_DELTA and CLK_ST231_AUD can also be divided on the fly without any change to the PLL1 setup.

PLL0 frequency change procedure

1. Write 0xC0DE in register CKGA_LCK.
2. Use the CKGA_PLL0_CFG register to move the clock-divider clock input from the PLL0 output to the SYSACLKIN input (set bit 20 to 1).
3. Disable the PLL0 (reset bit CKGA_PLL0_CFG.PLL0_EN).
4. Set new values in register CKGA_PLL0_CFG, fields PLL0_MDIV, PLL0_NDIV and PLL_PDIV.
5. Enable the PLL0 (set bit CKGA_PLL0_CFG.PLL0_EN).
6. Wait until the PLL locks by polling register CKGA_PLL0_STA.
7. Use register CKGA_PLL0_CFG to move the clock-divider clock input from the SYSACLKIN input to the PLL output (set bit 20 to 0).

PLL1 frequency change procedure

1. Use register CKGA_PLL1_BYPASS to bypass the PLL1 output and use the SYSACLKIN input (set bit 1 to 1).
2. Disable the PLL1 (reset bit PLL1_EN of register CKGA_PLL1_CFG).
3. Set new values in register CKGA_PLL1_CFG, fields PLL1_MDIV, PLL1_NDIV and PLL1_PDIV.
4. Enable the PLL1 (set bit CKGA_PLL1_CFG.PLL1_EN).
5. Wait until the PLL locks by reading register CKGA_PLL1_STA.
6. Use register CKGA_PLL1_CFG to use the PLL1 output instead of the SYSACLKIN input (set bits 20 to 0).

15.2.5 Clock slowing

Most group A clocks can be slowed to reduce power consumption without stopping the clocks.

The clocks CLK_SYS_LMI_2X, CLK_VID_LMI_2X, CLK_ST231_AUD and CLK_ST231_DELTA can be divided on the fly by 1024 using the register CKGA_CLK_DIV.

The clocks CLK_ST40_IC, CLK_ST40, CLK_FDMA and CLK_MPEG2 can be reduced using registers CKGA_PLL0_CLK1, CKGA_PLL0_CLK2, CKGA_PLL0_CLK3 and CKGA_PLL0_CLK4.

15.2.6 Clock stopping

The PLL0 clocks CLK_ST40 and CLK_ST40_IC can be stopped using the configuration register CKGA_CLK_EN.

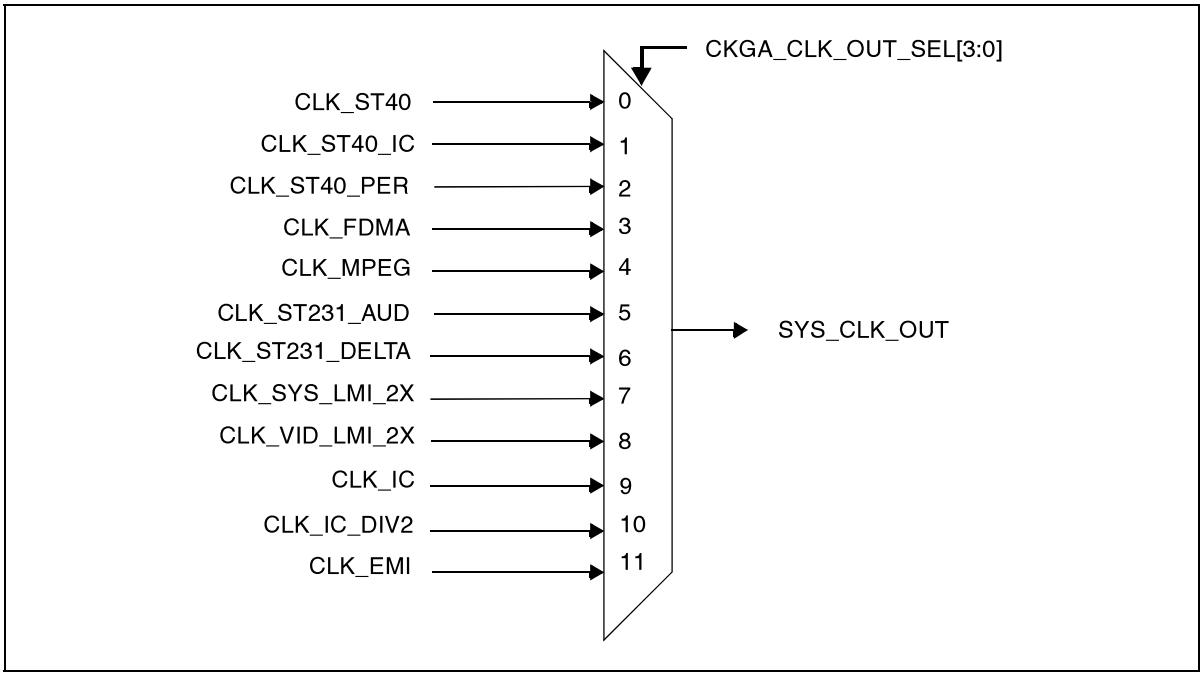
The PLL1 clocks CLK_ST231_AUD, CLK_ST231_DELTA, CLK_SYS_LMI_2X and CLK_VID_LMI_2X can be stopped using the configuration register CKGA_CLK_EN.

15.2.7 Clock observation

Any group A clock can be routed and observed on the SYS_CLK_OUT output pin.

The configuration register CKGA_CLK_OUT_SEL selects the clock to be routed to the pin.

Figure 51: PLL0 and PLL1 clocks observation



15.3 Clock generator B

This clock generator is mainly responsible for generating the clocks used by the video display pipeline. This includes the following units:

- SD and HD displays,
- compositor,
- video output stage (formatters, HDMI, DENC),
- HD and SD Video DACs.

In addition, clockgen B also generates some processing clocks for the following units:

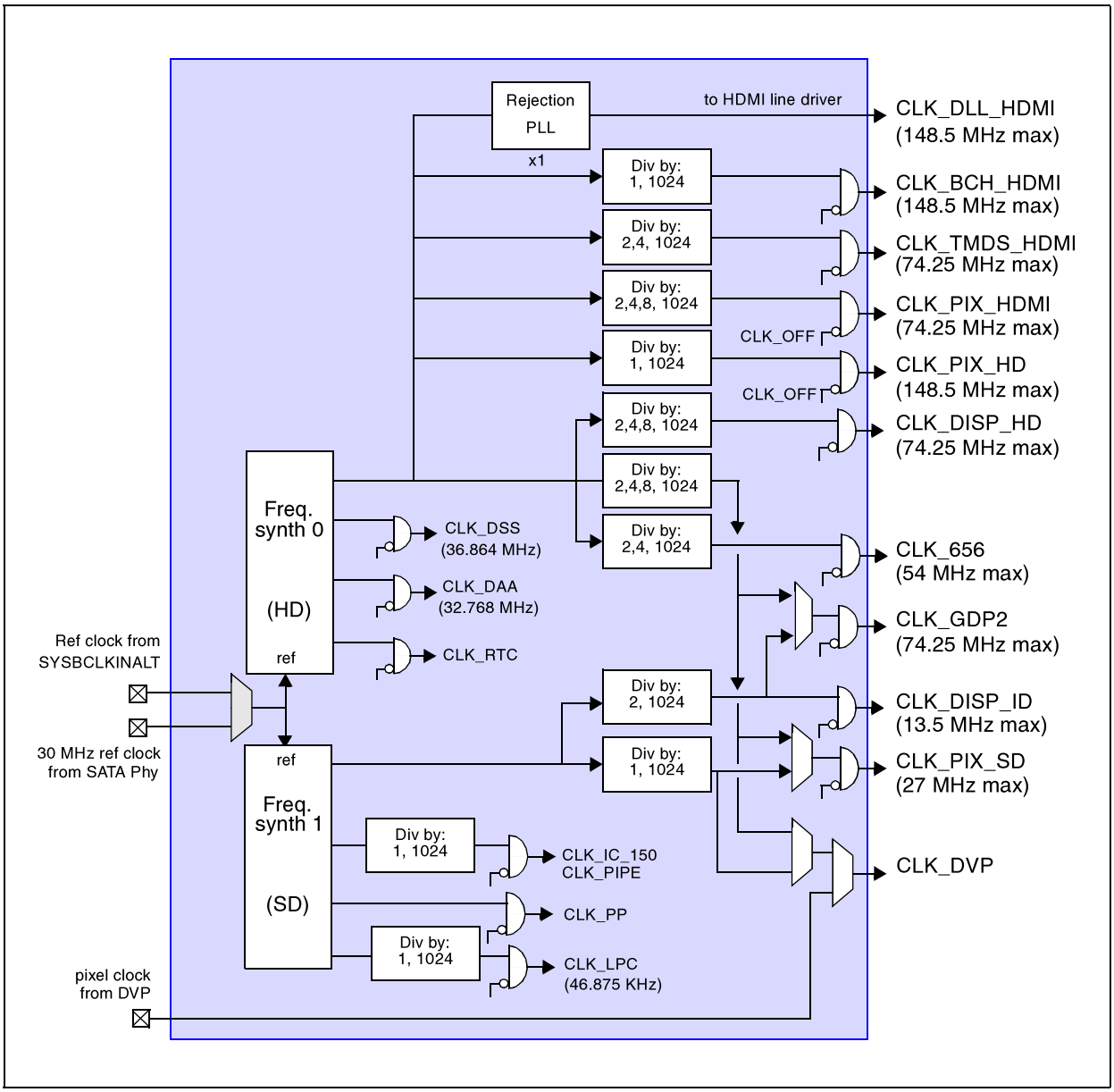
- MPEG2 video decoder,
- comms,
- Delta pre-processor,
- transport subsystem (PTI, CryptoCore, PDES and TSMerger).

Clockgen B comprises two digitally-controlled frequency synthesizers (FS0 and FS1). The reference clock can be either an internal 30 MHz clock signal or a clock connected to the SYSBCLKINALT pin. The selection is done with the configuration register CKGB_REF_CLK_SEL.

Clockgen B also includes a digital clock recovery module to recover the encoder clock.

15.3.1 Block diagram

Figure 52: Clockgen B block diagram



Note: CLK_RTC *has a hardware fixed frequency synthesizer setup. These settings are for a 30 MHz source clock.*

15.3.2 Clock signals

Table 68 lists group B clocks with their maximum frequencies.

Table 68: Clockgen B

Clock name	Maximum frequency (MHz)	Description
CLK_PIX_HD	148.5	HD pixel clock
CLK_PIX_SD	27	SD pixel clock
CLK_DISP_HD	74.25	HD display clock
CLK_DISP_ID	13.5	SD display clock
CLK_GDP2	74.25	GDP2 pixel clock (HD or SD)
CLK_656	54	DVO pixel clock
CLK_PIPE	150	Video pipeline processing clock
CLK_PP	150	Delta (H.264) pre-processor clock
CLK_IC_150	150	Interconnect clock 150 MHz
CLK_DAA	32.768	DAA clock
CLK_DSS	36.864	DSS clock
CLK_LPC		Low power controller (LPC) clock
CLK_TTXT	27	Teletext clock
CLK_SERLZR_HDMI	148.5	HDMI serializer clock
CLK_BCH_HDMI	148.5	HDMI BCH clock
CLK_TMDS_HDMI	74.25	HDMI TMDS clock
CLK_PIX_HDMI	74.25	HDMI pixel clock

The frequency of all clocks is programmable. The video clocks are particularly critical, since they must be setup with respect to the display standard in use.

Table 69 gives some programming examples with respect to the targeted application.

Table 69: Video displays clocking for various application

Clock signal	HD on main, SD on aux (GDP2 on main)	HD on main, SD on aux (GDP2 on aux)	SD progressive on main, SD interleaved on aux (GDP2 on main)	SD progressive on main, SD interleaved on aux (GDP2 on aux)	SD interleaved on main only
CLK_PIX_HD	148.5	148.5	108	108	108
CLK_DISP_HD	74.25	74.25	27	27	13.5
CLK_GDP2	74.25	13.5	27	13.5	13.5
CLK_PIX_SD	27	27	27	27	27 (from HD)
CLK_DISP_ID	13.5	13.5	13.5	13.5	Not used
CLK_656	Not used	Not used	54	54	27
CLK_DISP_HDMI	74.25	74.25	27	27	13.5
CLK_TMDS_HDMI	74.25	74.25	27	27	27
CLK_BCH_HDMI	148.5	148.5	108	108	108
CLK_DLL_HDMI	148.5	148.5	108	108	108

15.3.3 Startup configuration

After the reset phase, clockgen B is by default configured with a 13.5 MHz display clock on both the main and auxiliary video outputs.

Table 70: Clockgen B default configuration

Clock name	Frequency (MHz)	Description
CLK_PIX_HD	108	HD pixel clock
CLK_PIX_SD	27	SD pixel clock
CLK_DISP_HD	13.5	HD display clock
CLK_DISP_ID	13.5	SD display clock
CLK_GDP2	13.5	GDP2 pixel clock (HD or SD)
CLK_656	27	DVO pixel clock
CLK_PIPE	150	Video pipeline processing clock
CLK_PP	150	Delta (H.264) pre-processor clock
CLK_IC_150	150	Interconnect clock 150 MHz
CLK_DAA	32.768	DAA clock
CLK_DSS	36.864	DSS clock
CLK_LPC		Low power controller clock
CLK_TTXT	27	Teletext clock
CLK_SERLZR_HDMI	108	HDMI serializer clock
CLK_BCH_HDMI	108	HDMI BCH clock
CLK_TMDS_HDMI	27	HDMI TMDS clock
CLK_PIX_HDMI	13.5	HDMI pixel clock

15.3.4 Clock frequency change

The clock generator always starts with the default configuration defined above. Nevertheless the frequency synthesizers FS0 and FS1 can be re-configured to produce different frequencies.

Clockgen programming: lock/unlock

To prevent any unwanted clockgen reprogramming, the CKGB_LCK register provides a protection mechanism. This register must be written first with the keyword “0xC0DE” to authorize any clockgen registers update. Writing any other value locks all clockgen B registers.

Clock ratio change without changing FS0 and FS1 programming

The clocks CLK_BCH_HDMI, CLK_TMDS_HDMI, CLK_PIX_HDMI, CLK_PIX_HD, CLK_DISP_HD, CLK_656, CLK_GDP2, CLK_DISP_ID and CLK_PIX_SD are generated from a master clock (from FS0 and FS1) which is then divided by programmable dividers (set to 2, 4, 8 or 1024). These dividers can be redefined on the fly via the register CKGB_DISP_CFG without changing the FS0 and FS1 setup. The clockgen design ensures a glitch-free frequency change.

FS0 and FS1 frequency definition

The frequencies generated by FS0 and FS1 are defined by the registers CKGB_FS0/1_MDx, CKGB_FS0/1_PEx and CKGB_FS0/1_SDIVx and are given by the formula:

$$F_{OUT} = \frac{2^{15} \cdot F_{PLL}}{2^{(sdiv+1)} \times \left[\left(pe \cdot \left(1 + \frac{(md-32)}{32}\right)\right) - \left((pe - 2^{15}) \cdot \left(1 + \frac{(md-31)}{32}\right)\right)\right]}$$

with F_{PLL} = 216 MHz if the reference clock is 27 MHz or F_{PLL} = 240 MHz if the reference clock is 30 MHz.

The MD, PE and PRG_EN parameters can be changed without creating glitches at the frequency synthesizer output. Changing other parameters may cause glitches.

Procedure to change FS0 and FS1 frequency

1. Write 0xC0DE in register CKGB_LCK.
2. Set CKGB_FS0_PRG_ENx to 0.
3. Define CKGB_FS0_MDx, CKGB_FS0_PEx, CKGB_FS0_SDIVx for the targeted frequency.
4. Set CKGB_FS0_PRG_ENx to 1 to validate the new values.
5. Set CKGB_FS0_PRG_ENx to 0.

15.3.5 Clock slowing

Most group B clocks can be divided to reduce power consumption with the register CKGB_CLK_DIV without stopping the clocks.

15.3.6 Clock stopping

The PLL0 clocks CLK_ST40, CLK_ST40_IC can be stopped using the configuration register CKGA_CLK_EN.

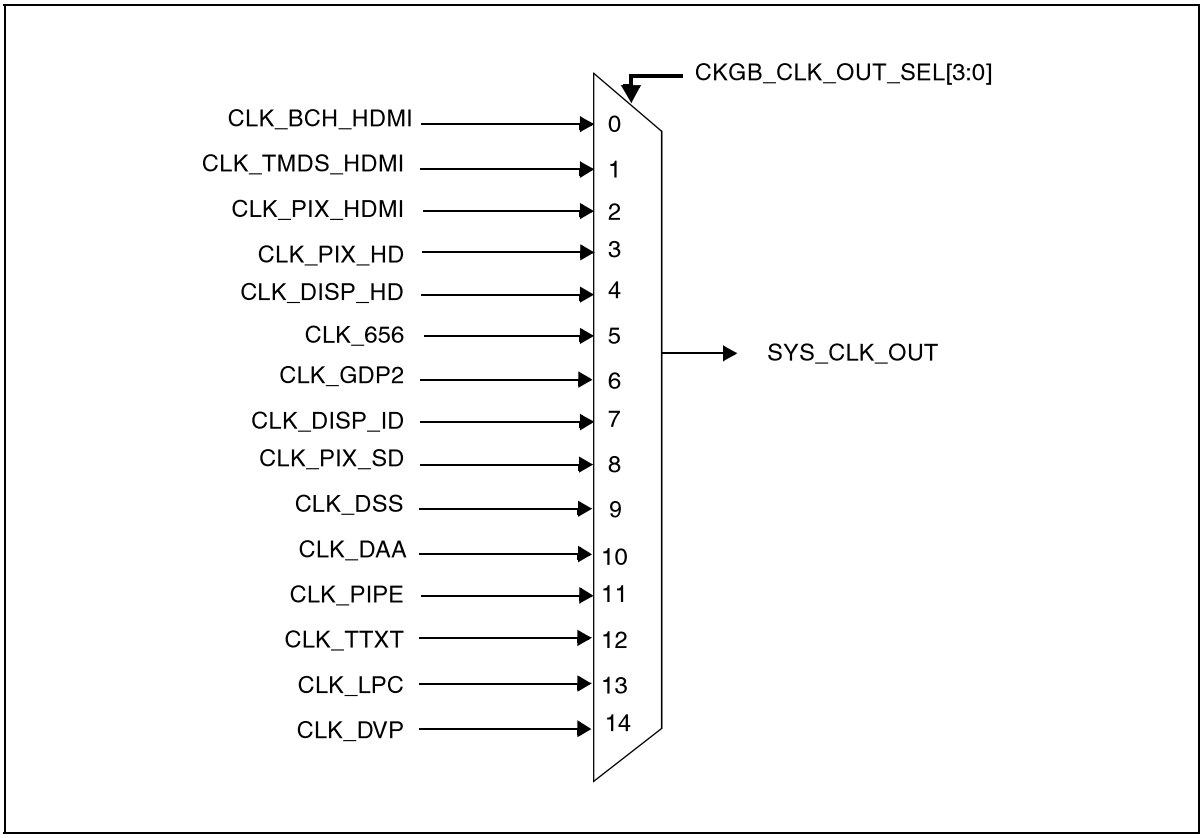
The PLL1 clocks CLK_ST231_AUD, CLK_ST231_DELTA, CLK_SYS_LMI_2X and CLK_VID_LMI_2X can be stopped using the configuration register CKGA_CLK_EN.

15.3.7 Clock observation

Any group B clock can be routed and observed on the alternate PIO5[2] output pin.

The configuration register CKGB_CLKOUT_SEL selects the clock to be routed to the pad.

Figure 53: FS0 and FS1 clocks observation



15.3.8 Clock recovery

The clock recovery is a mechanism to adjust the locally generated clocks with the encoder clock referenced in the PCR (program counter reference) located in the adaptation field of the incoming transport stream.

The STx7100 generates three local clocks from internal frequency synthesizers using a fixed and stable 27 or 30 MHz reference clock.

These three clocks are:

- CLK_PIX_SD used for SD display generated from FS0,
- CLKL_PIX_HD used for HD display generated from FS1,
- CLK_PCM used for audio output generated from FS2.

Clock recovery principle

The mechanism assumes that these three clocks are related one to the others.

The recovery is done as usual for the CLK_PIX_SD (generated from the frequency synthesizer FS0) by comparing the 42-bits PCR value located in the adaptation field of the stream with the local STC (system timer counter clocked by CLK_PIX_SD) value when a packet arrived. This generates a potential correction that is applied to the frequency synthesizer FS0 to adjust the CLK_PIX_SD clock. The frequency synthesizer is programmed with new setup values to slow or accelerate the clock.

For audio PCM clock recovery, two counters are used:

- a PCM free-running counter clocked by the audio frequency synthesizer FS2,
- a reference counter clocked by the SD video frequency synthesizer FS0. The maximum value of this counter is programmable defining the time interval between two consecutive resets. This counter is used as a time-base.

When the reference counter resets, the values of the free-running counter clocked by CLK_PCM is captured into a readable register. This event generates an interrupt to the CPU (CRU_IRQ). The CPU reads the value and compares it with the previously captured value. The difference between two adjacent values gives an indication of the correction to apply to the PCM audio frequency synthesizer FS2.

The decision to correct the frequency synthesizers setup is under the control of the software.

The same principle applies for the recovery of the CLK_PIX_HD. A free-running counter is clocked from the HD video frequency synthesizer FS1. The same reference counter is used. When this counter resets, then the output of the free-running counter clocked by CLK_PIX_HD is captured into a readable register.

Clock recovery commands

The clock recovery module accepts a single command defined by register field CKGB_CRU_CMD.ID.

When set to 1, this command loads the reference counter with the value defined in the register CKGB_REF_MAX, resets the PCM counter and HD Video counter. Resetting this command to 0 starts the counters.

Clock recovery interrupt

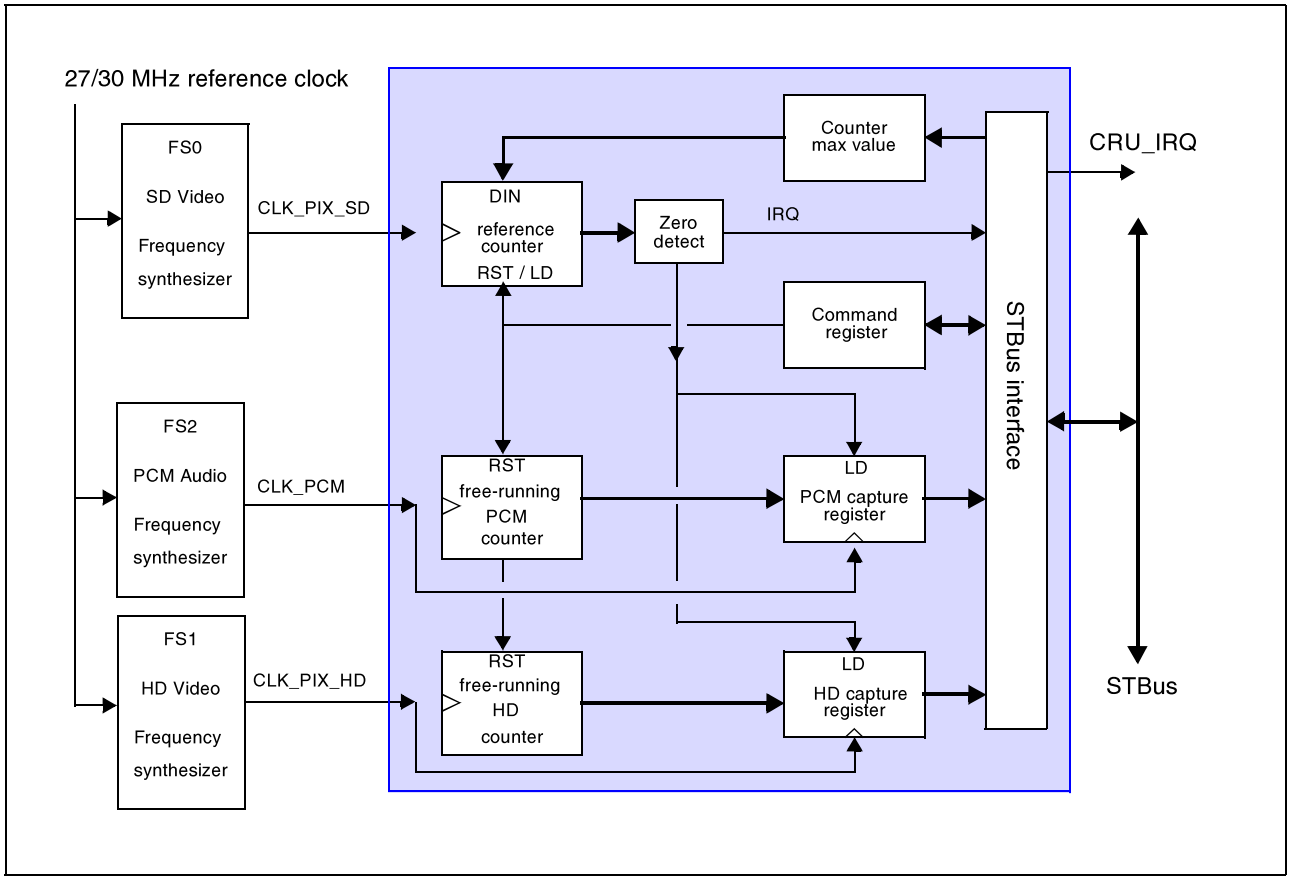
An interrupt line is available, generated by the clock recovery unit. The interrupt is asserted when the reference counter clocked at CLK_PIX_SD resets.

This interrupt status is captured in the CMD register and is cleared only when a 1 is written to bitfield CKGB_CRU_CMD.INT. Writing 0 enables new interrupts.

Block diagram

The clock recovery unit (CRU) block diagram is described in Figure 54.

Figure 54: Clock recovery unit block diagram



16 Clock registers

16.1 Summary

Register addresses are provided as:

ClkABaseAddress + offset or *ClkBBaseAddress* + offset.

The *ClkABaseAddress* is:

0x1921 3000

The *ClkBBaseAddress* is:

0x1900 0000.

Table 71: Clock generator A register summary

Name	Function	Offset	Reset value	Type
CKGA_LCK	Clockgen A lock	0x000	0x0000 0000	R/W
CKGA_MD_STA	Mode pins status	0x004	from mode pins	RO
CKGA_PLL0_CFG	PLL0 configuration	0x008	from mode pins	Mixed
Reserved	Reserved	0x00C	-	-
CKGA_PLL0_LCK_STA	PLL0 lock status	0x010	Undefined	RO
CKGA_PLL0_CLK1	CLK_ST40 ratio	0x014	0x0000 0000	R/W
CKGA_PLL0_CLK2	CLK_ST40_IC ratio	0x018	0x0000 0001	
CKGA_PLL0_CLK3	CLK_ST40_PER ratio	0x01C	0x0000 0000	
CKGA_PLL0_CLK4	CLK_FDMA ratio	0x020	0x0000 0000	
CKGA_PLL1_CFG	PLL1 configuration	0x024	From mode pins	
Reserved	Reserved	0x028	-	-
CKGA_PLL1_LCK_STA	PLL1 lock status	0x02C	Undefined	RO
CKGA_CLK_DIV	Clocks division	0x030	0x0000 0000	R/W
CKGA_CLK_EN	Clocks enabling/stopping	0x034	0x0000 003f	
CKGA_CLKOUT_SEL	SYSCLKOUT clock source selection	0x038	0x0000 0000	
CKGA_PLL1_BYPASS	PLL1 bypass and FDMA clock source	0x03C	From mode pins	

Table 72: Clock generator B register summary

Name	Function	Offset	Reset value	Type
Clock recovery				
CKGB_REF_MAX	Max value for CRU reference counter	0x000	0x0000 0000	R/W
CKGB_CMD	CRU command register	0x004	0x0000 0001	
CKGB_CPT_PCM	CRU captured audio PCM counter value	0x008	0x0000 0000	
CKGB_CPT_HD	CRU captured HD video counter value	0x00C	0x0000 0000	
Configuration				
CKGB_LCK	Clockgen B lock	0x010	0x0000 0000	R/W
CKGB_FS0_CFG	Global FS0 parameters	0x014	0x0000 0018	
CKGB_FS0_MD1	FS0 channel 1 coarse selection	0x018	0x0000 0011	
CKGB_FS0_PE1	FS0 channel 1 fine selection	0x01C	0x0000 1C72	
CKGB_FS0_PRG_EN1	FS0 channel 1 programming enable	0x020	0x0000 0001	
CKGB_FS0_SDIV1	FS0 channel 1 output clock divider	0x024	0x0000 0001	

Table 72: Clock generator B register summary

Name	Function	Offset	Reset value	Type
CKGB_FS0_MD2	FS0 channel 2 coarse selection	0x028	0x0000 001A	R/W
CKGB_FS0_PE2	FS0 channel 2 fine selection	0x02C	0x0000 7AAB	
CKGB_FS0_PRG_EN2	FS0 channel 2 programming enable	0x030	0x0000 0001	
CKGB_FS0_SDIV2	FS0 channel 2 output clock divider	0x034	0x0000 0002	
CKGB_FS0_MD3	FS0 channel 3 coarse selection	0x038	0x0000 001D	
CKGB_FS0_PE3	FS0 channel 3 fine selection	0x03C	0x0000 5A00	
CKGB_FS0_PRG_EN3	FS0 channel 3 programming enable	0x040	0x0000 0001	
CKGB_FS0_SDIV3	FS0 channel 3 output clock divider	0x044	0x0000 0002	
Reserved	-	0x048 - 0x054	-	-
CKGB_FS0_PWR_DN	FS1 digital part power-down/up	0x058	0x0000 0077	R/W
CKGB_FS1_CFG	Global FS1 parameters	0x05C	0x0000 0018	
CKGB_FS1_MD1	FS1 channel 1 coarse selection	0x060	0x0000 0011	
CKGB_FS1_PE1	FS1 channel 1 fine selection	0x064	0x0000 1C72	
CKGB_FS1_PRG_EN1	FS1 channel 1 programming enable	0x068	0x0000 0001	
CKGB_FS1_SDIV1	FS1 channel 1 output clock divider	0x06C	0x0000 0003	
CKGB_FS1_MD2	FS1 channel 2 coarse selection	0x070	0x0000 0019	
CKGB_FS1_PE2	FS1 channel 2 fine selection	0x074	0x0000 3333	
CKGB_FS1_PRG_EN2	FS1 channel 2 programming enable	0x078	0x0000 0001	
CKGB_FS1_SDIV2	FS1 channel 2 output clock divider	0x07C	0x0000 0000	
CKGB_FS1_MD3	FS1 channel 3 coarse selection	0x080	0x0000 0011	
CKGB_FS1_PE3	FS1 channel 3 fine selection	0x084	0x0000 1C72	
CKGB_FS1_PRG_EN3	FS1 channel 3 programming enable	0x088	0x0000 0001	
CKGB_FS1_SDIV3	FS1 channel 3 output clock divider	0x08C	0x0000 0003	
CKGB_FS1_MD4	FS1 channel 4 coarse selection	0x090	0x0000 0013	
CKGB_FS1_PE4	FS1 channel 4 fine selection	0x094	0x0000 0000	
CKGB_FS1_PRG_EN4	FS1 channel 4 programming enable	0x098	0x0000 0001	
CKGB_FS1_SDIV4	FS1 channel 4 output clock divider	0x09C	0x0000 0002	
CKGB_FS1_PWR_DN	FS1 digital part power-down/up	0x0A0	0x0000 00FF	
CKGB_DISP_CFG	Video display clocks configuration	0x0A4	0x0000 0469	
CKGB_CLK_SRC	Clock source selection	0x0A8	0x0000 0006	
CKGB_CLK_DIV	Individual clocks division	0x0AC	0x0000 0200	
CKGB_CLK_EN	Individual clocks enable	0x0B0	0x0000 3FFF	
CKGB_CLKOUT_SEL	Clocks observation selection	0x0B4	0x0000 0000	
CKGB_REF_CLK_SEL	Reference clock source selection	0x0B8	0	

16.2 Clock generator A

CKGA_LCK Clockgen A lock

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																LCK															

Address: *ClkABaseAddress* + 0x000
Type: R/W
Reset: 0
Description: Must be written with the value 0xC0DE to write to any clockgen A configuration register.

CKGA_MD_STA Mode pins status

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												MD			

Address: *ClkABaseAddress* + 0x004
Type: RO
Reset: Captured during reset
Description: Reports the status of the mode pins captured during the power-on-reset.

[31:4] **Reserved**

[3:2] **MD[3:2]**: PLL1 startup configuration

[1:0] **MD[1:0]**: PLL0 startup configuration

CKGA_PLL0_CFG PLL0 configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											PLL0_BYPASS	PLL0_EN	PLL0_PDIV			PLL0_NDIV								PLL0_MDIV							

Address: *ClkABaseAddress* + 0x008

Type: R/W

Reset: See Table 73 and Table 74.

Description: Defines the PLL0 setup. The reset values are function of the mode pins values captured during the reset.

[31:21] **Reserved**
Bit 21 must be set to 0.

[20] **PLL0_BYPASS**
0: PLL0 output clock is used
1: PLL0 is bypass - SYSACLIN clock is used

[19] **PLL0_EN**: PLLO enable
0: PLL0 is in power-down mode
1: PLL0 is enabled

[18:16] **PLL0_PDIV**: '2^P' post-divider ratio - from 1 to 32

[15:8] **PLL0_NDIV**: N feedback divider ratio - from 3 to 255

[7:0] **PLL0_MDIV**: M pre-divider ratio - from 1 to 255

The reset values of CKGA_PLL0_CFG depends on MD[1:0], as described in Table 73 and Table 74.

Table 73: PLL0_CFG reset values

MD[1:0]	MDIV	NDIV	PDIV	Enable	PLL0 CLKOUT (MHz)
00	0x06 (6)	0x3B (59)	0x0	1	531
01	0x1B (27)	0xC8 (200)	0x0	1	400
10	0x06 (6)	0x3B (59)	0x0	0	27 (PLL bypassed)
11	0x09 (9)	0x64 (100)	0x0	1	600

Table 74: PLL0_CFG reset values

MD[1:0]	bit 21	PLL0 bypass	PLL0 enable	Description
00	0	0	1	PLL0_CLKOUT selected - PLL0 on
01	0	0	1	PLL0_CLKOUT selected - PLL0 on
10	0	1	0	SYSA_CLK_IN selected - PLL0 off
11	0	0	1	PLL0_CLKOUT selected - PLL0 on

The PLL0 frequency is given by the formula:

$$F_{PLL0} = \frac{2 \times N \times F_{sysaclkin}}{M \times 2^{P}}$$

with:

N in the interval [3, 255],

M in the interval [1, 255],

P in the interval [1, 32].

CKGA_PLL0_LCK_STA PLL0 lock status

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															LCK

Address: *ClkABaseAddress* + 0x010

Type: RO

Reset: Undefined

Description: Describes the lock status of the PLL0.

0: PLL0 is unlocked
1: PLL0 is locked

CKGA_PLL0_CLK1 CLK_ST40 ratio

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														RATIO	

Address: *ClkABaseAddress* + 0x014

Type: R/W

Reset: 0

Description: Defines the clock ratio of the CLK_ST40 clock (PLL1_CLK1) with respect to the PLL0 output clock.

000: Ratio 1:1
001: Ratio 1:2
010: Ratio 1:3
011: Ratio 1:4
100: Ratio 1:6
101: Ratio 1:8
110: Ratio 1:1
111: Ratio 1:1

CKGA_PLL0_CLK2 CLK_ST40 IC ratio

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																													RATIO		

Address: *ClkABaseAddress* + 0x018

Type: R/W

Reset: 0

Description: Defines the clock ratio of the CLK_ST40_IC clock (PLL1_CLK2) with respect to the PLL0 output clock (MAIN_CLOCK).

000: Ratio 1:1
001: Ratio 1:2
010: Ratio 1:3
011: Ratio 1:4
100: Ratio 1:6
101: Ratio 1:8
110: Ratio 1:2
111: Ratio 1:2

CKGA_PLL0_CLK3 CLK_ST40_PER ratio

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																													RATIO		

Address: *ClkABaseAddress* + 0x01C

Type: R/W

Reset: 0

Description: Defines the clock ratio of the CLK_ST40_PER clock (PLL1_CLK3) with respect to the PLL0 output clock (MAIN_CLOCK).

000: Ratio 1:4
001: Ratio 1:2
010: Ratio 1:4
011: Ratio 1:4
100: Ratio 1:6
101: Ratio 1:8
110: Ratio 1:4
111: Ratio 1:4

CKGA_PLL0_CLK4 CLK_FDMA ratio

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																													RATIO		

Address: *ClkABaseAddress* + 0x020

Type: R/W

Reset: 0

Description: Defines the clock ratio of the CLK_FDMA clock (PLL1_CLK4[1]) with respect to the PLL0 output clock (MAIN_CLOCK).

000: Ratio 1:1
001: Ratio 1:2
010: Ratio 1:3
011: Ratio 1:4
100: Ratio 1:6
101: Ratio 1:8
110: Ratio 1:3
111: Ratio 1:3

1. Also used for CLK_MPEG2

CKGA_PLL1_CFG PLL1 configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												PLL1_EN	PLL1_PDIV			PLL1_NDIV								PLL1_MDIV							

Address: *ClkABaseAddress* + 0x024

Type: R/W

Reset: See Table 75

Description: Defines PLL1 setup. The reset values are functions of the mode pins values captured during the reset.

[31:20] **Reserved**

[19] **PLL1_EN**: PLL1 enable
0: PLL is in power-down mode.
1: PLL is on.

[18:16] **PLL1_PDIV**: '2^P' post-divider ratio - from 1 to 32

[15:8] **PLL1_NDIV**: N feedback divider ratio - from 1 to 255

[7:0] **PLL1_MDIV**: M pre-divider ratio - from 1 to 255

The reset values of PLL1_CFG fields depends on MD[2:0] as described in Table 75.

Table 75: PLL1_CFG startup values

MD[3:2]	MDIV	NDIV	PDIV	Enable	PLL1_CLKOUT (MHz)
00	0x1B (27)	0xC8	0x0	1	400
01	0x03 (3)	0x25	0x1	1	333
10	0x1B (27)	0x85	0x0	1	266
11	0x06 (6)	0x3B	0x0	0	27 (PLL bypassed)

The PLL1 frequency is given by the formula:

$$F_{PLL1} = \frac{2 \times N \times F_{sysaclkin}}{M \times P}$$

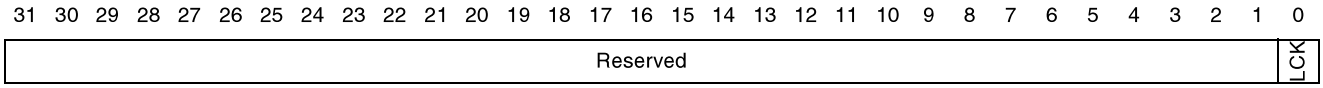
with:

N in the interval [3, 255],

M in the interval [1, 255],

P in the interval [1, 32].

CKGA_PLL1_LCK_STA PLL1 lock status



Address: *ClkABaseAddress* + 0x02C

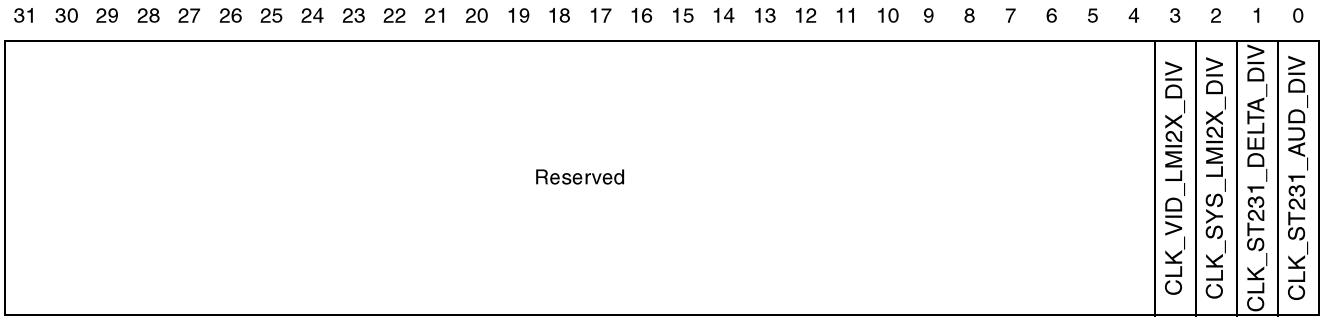
Type: RO

Reset: Undefined

Description: Describes the lock status of PLL1.

0: PLL1 is unlocked
1: PLL1 is locked

CKGA_CLK_DIV Clocks division



Address: *ClkABaseAddress* + 0x030

Type: R/W

Reset: 0

Description: Allows some of the clocks generated from the PLL1 to be reduced in frequency. Can be used to minimize power consumption without stopping the clocks.

[31:4] **Reserved**

[3] **CLK_VID_LMI2X_DIV**
0: Nominal frequency value
1: CLK_VID_LMI_2X clock is divided by 1024

[2] **CLK_SYS_LMI2X_DIV**
0: Nominal frequency value
1: CLK_SYS_LMI_2X clock is divided by 1024

[1] **CLK_ST231_DELTA_DIV**
0: Nominal frequency value
1: CLK_ST231_DELTA clock is divided by 1024

[0] **CLK_ST231_AUD_DIV**
0: Nominal frequency value
1: CLK_ST231_AUD clock is divided by 1024

CKGA_CLK_EN Clocks enabling/stopping

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										CLK_LMI2X_VID_EN	CLK_LMI2X_SYS_EN	CLK_ST40_IC_EN	CLK_ST40_EN	CLK_ST231_DELTA_EN	CLK_ST231_AUD_EN

Address: *ClkABaseAddress* + 0x034

Type: R/W

Reset:

Description: Switches on or off a number of clocks generated from PLL0 and PLL1.

[31:6] **Reserved**

[5] **CLK_LMI2X_VID_EN**: CLK_LMI_2X_VID clock enable
0: Stop 1: Enable

[4] **CLK_LMI2X_SYS_EN**: CLK_LMI_2X_SYS clock
0: Stop 1: Enable

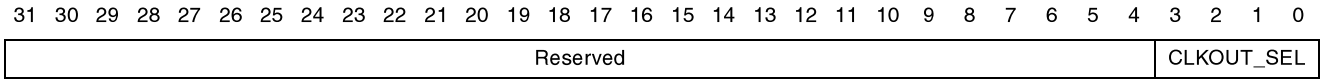
[3] **CLK_ST40_IC_EN**: CLK_ST40_IC clock
0: Stop 1: Enable

[2] **CLK_ST40_EN**: CLK_ST40 clock enable
0: Stop 1: Enable

[1] **CLK_ST231_DELTA_EN**: CLK_ST231_DELTA clock enable
0: Stop 1: Enable

[0] **CLK_ST231_AUD_EN**: CLK_ST231_AUD clock enable
0: Stop 1: Enable

CKGA_CLKOUT_SEL SYSCLKOUT clock source selection



Address: *ClkABaseAddress* + 0x038

Type: R/W

Reset: 0

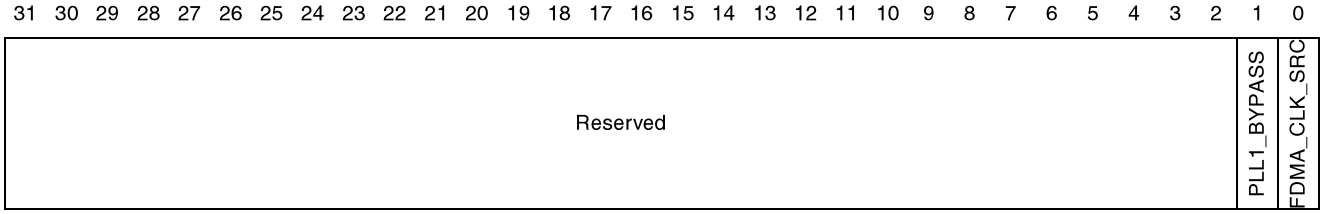
Description: Selects which clock of clockgen A to be routed to the SYSCLKOUT pin.

Table 76: SYSCLOUT pin source

CLKOUT_SEL	SYSCLKOUT
0000	CLK_ST40
0001	CLK_ST40_IC
0010	CLK_ST40_PER
0011	CLK_FDMA
0100	CLK_MPEG
0101	CLK_ST231_AUD
0110	CLK_ST231_DELTA
0111	CLK_SYS_LMI_2X

CLKOUT_SEL	SYSCLKOUT
1000	CLK_VID_LMI_2X
1001	CLK_IC
1010	CLK_IC_DIV2
1011	CLK_EMI
1100 to 1111	Reserved
1101	
1110	
1111	

CKGA_PLL1_BYPASS PLL1 bypass and FDMA clock source



Address: *ClkABaseAddress* + 0x03C

Type: R/W

Reset: See below

Description: Provides a control bit (PLL1_BYPASS) to bypass the PLL1 output clock and to use the clock driving the SYSACLKIN input pin (usually 27 MHz). This feature must be used when changing the PLL1 configuration.

The bit FDMA_CLK_SRC allows selection of either PLL0 (default) or PLL1 as a clock source.

[31:2] **Reserved**

[1] **PLL1_BYPASS**
0: PLL1_CLKOUT is used
1: PLL1_CLKOUT is bypassed and SYSA_CLK_IN clock is used instead
Reset: From mode pins

[0] **FDMA_CLK_SRC**
0: PLL0 is the PLL source for CLK_FDMA
1: PLL1 is the source PLL for CLK_FDMA
Reset: 0

16.3 Clock generator B

CKGB_REF_MAX Max value for CRU reference counter

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REF_MAX																															

Address: *ClkBBaseAddress* + 0x000

Type: R/W

Reset: 0

Description: Load value of the reference counter for the video clock recovery. The reference counter resets each time it reaches this value.

CKGB_CRU_CMD CRU command

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																														INT	LD

Address: *ClkBBaseAddress* + 0x004

Type: R/W

Reset: 0x01

Description: Holds the load command that can be applied to the clock recovery unit.

When the load command is set to ‘1’ the reference counter is loaded with REF_MAX, PCM and HD counters are reset to zero.

When the load command is reset to ‘0’, this starts the count.

This register also holds the interrupt status. When written to, the interrupt is cleared.

The counters and interrupt generation can be stopped by setting LD to ‘1’ after a clear interrupt has occurred.

[31:2] **Reserved**

[1] **INT**

Read: get the interrupt status

1: interrupt has occurred and the counters can be read

0: no interrupt

Write:

1: clear the current interrupt

0: allows the next interrupt to occur

[0] **LD**

0: start the counters

1: reset the counters and load the REF_MAX value

CKGB_CPT_PCM CRU captured audio PCM counter value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPT_PCM																															

Address: *ClkBBaseAddress* + 0x008
Type: R/W
Reset: 0
Description: Value captured at the output of the PCM counter when an interrupt has occurred.

CKGB_CPT_HD CRU captured HD video counter value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CPT_HD																															

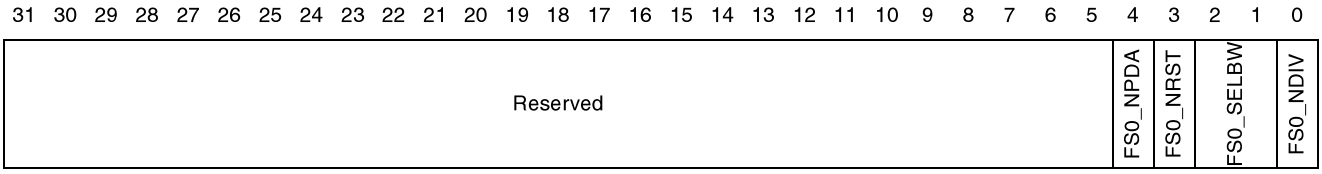
Address: *ClkBBaseAddress* + 0x00C
Type: R/W
Reset: 0
Description: Value captured at the output of the HD counter when an interrupt has occurred.

CKGB_LCK Clockgen B lock

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																LCK															

Address: *ClkBBaseAddress* + 0x010
Type: R/W
Reset: 0
Description: Must be written with the value 0xC0DE to access any clockgen B configuration register.

CKGB_FS0_CFG Global FS0 parameters



Address: *ClkBBaseAddress* + 0x014

Type: R/W

Reset: 0x0018

Description: Defines the FS0 frequency synthesizer global parameters.

[31:5] **Reserved**

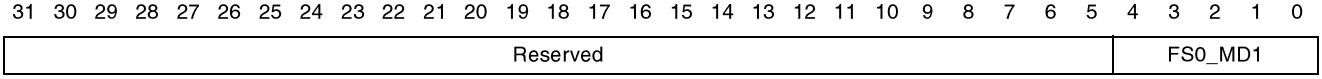
[4] **FS0_NPDA**: Analog power down mode
0: Analog power down
1: Analog power up

[3] **FS0_NRST**: Software reset
0: Reset active
1: Running

[2:1] **FS0_SELBW**: Bandwidth selection for ref clock noise reduction
00: Good reference (bandwidth = 2.4 MHz)
01: Very bad reference (bandwidth = 0.8 MHz)
10: Bad reference (bandwidth = 1.2 MHz)
11: Very good reference (bandwidth = 4 MHz)

[0] **FS0_NDIV**: Select the input frequency, if NDIV is set to
0: Ref clock frequency must be 27/30 MHz
1: Ref clock frequency must be 54/60 MHz

CKGB_FS0_MD1 FS0 channel 1 coarse selection



Address: *ClkBBaseAddress* + 0x018

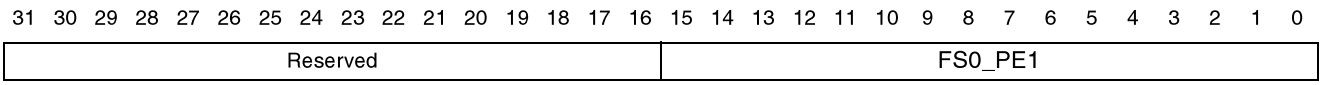
Type: R/W

Reset: 0x0011

Description: Defines the MD1 parameter (coarse selection) for the frequency synthesizer FS0 channel 1.

The MD1 reset value is defined to generate a frequency of 108 MHz on CLK_PIX_HD.

CKGB_FS0_PE1 FS0 channel 1 fine selection



Address: *ClkBBaseAddress* + 0x01C

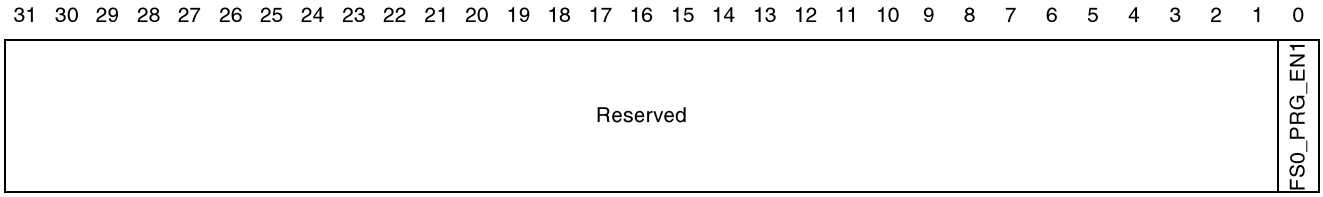
Type: R/W

Reset: 0x1C72

Description: Defines the PE1 parameter (fine selection) for the frequency synthesizer FS0 channel 1.

The PE1 reset value is defined to generate a frequency of 108 MHz on CLK_PIX_HD.

CKGB_FS0_PRG_EN1 FS0 channel 1 programming enable



Address: *ClkBBaseAddress* + 0x020

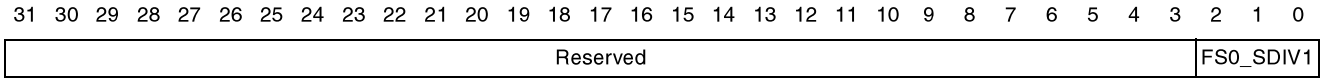
Type: R/W

Reset: 0x01

Description: Defines the PRG_EN parameter (programming enable) for the frequency synthesizer FS0 channel 1. This parameter must be set to 1 to take into account a new configuration.

0: PE1 and MD1 parameters are ignored
1: PE1 and MD1 parameters are taken into account

CKGB_FS0_SDIV1 FS0 channel 1 output clock divider



Address: *ClkBBaseAddress* + 0x024

Type: R/W

Reset: 0x01

Description: Defines the SDIV1 parameter (output divider control) for the frequency synthesizer FS0 channel 1, from 1 to 256.

The SDIV1 reset value is defined to generate a frequency of 108 MHz on CLK_PIX_HD.

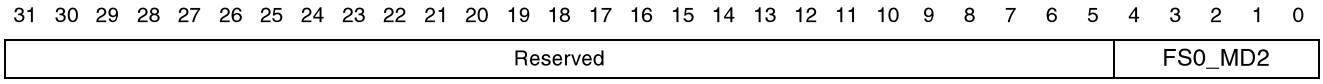
To generate a frequency of 148.5 MHz the following parameters can be used:

SDIV1 = 0x0

MD1 = 0x19

PE1 = 0x121A

CKGB_FS0_MD2 FS0 channel 2 coarse selection



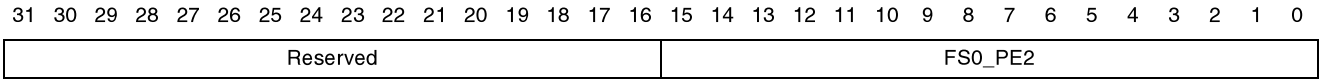
Address: *ClkBBaseAddress* + 0x028

Type: R/W

Reset: 0x001A

Description: Defines the MD2 parameter (coarse selection) for the frequency synthesizer FS0 channel 2.

CKGB_FS0_PE2 FS0 channel 2 fine selection



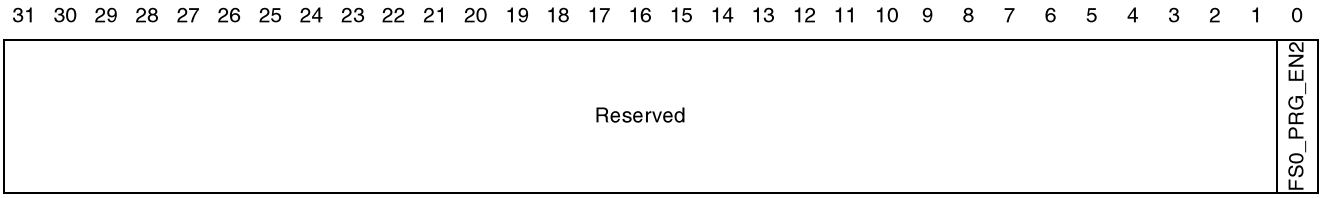
Address: *ClkBBaseAddress* + 0x02C

Type: R/W

Reset: 0x7AAB

Description: Defines the MD2 parameter (fine selection) for the frequency synthesizer FS0 channel 2.

CKGB_FS0_PRG_EN2 FS0 channel 2 programming enable



Address: *ClkBBaseAddress* + 0x030

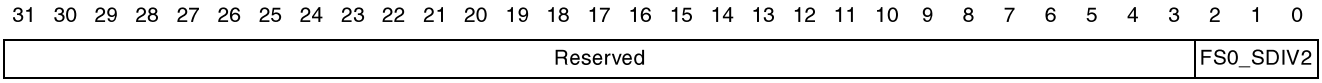
Type: R/W

Reset: 0x01

Description: Defines the PRG_EN parameter (programming enable) for the frequency synthesizer FS0 channel 2. This parameter must be set to 1 to take into account a new configuration.

0: PE2 and MD2 parameters are ignored
1: PE2 and MD2 parameters are taken into account

CKGB_FS0_SDIV2 FS0 channel 2 output clock divider



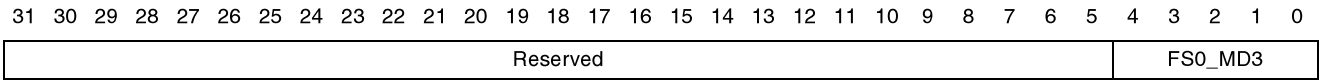
Address: *ClkBBaseAddress* + 0x034

Type: R/W

Reset: 0x02

Description: Defines the SDIV2 parameter (output divider control) for the frequency synthesizer FS0 channel 2; allowed values are from 2 to 256.

CKGB_FS0_MD3 FS0 channel 3 coarse selection



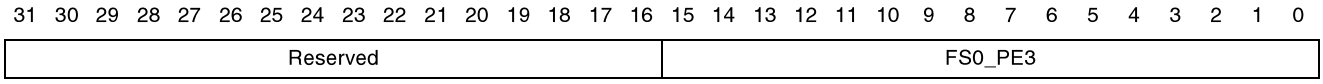
Address: *ClkBBaseAddress* + 0x038

Type: R/W

Reset: 0x1D

Description: Defines the MD3 parameter (coarse selection) for the frequency synthesizer FS0 channel 3.

CKGB_FS0_PE3 FS0 channel 3 fine selection



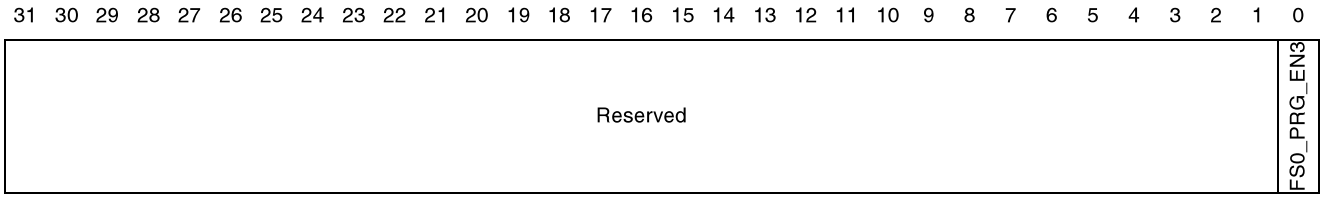
Address: *ClkBBaseAddress* + 0x03C

Type: R/W

Reset: 0x5A00

Description: Defines the MD3 parameter (fine selection) for the frequency synthesizer FS0 channel 3.

CKGB_FS0_PRG_EN3 FS0 channel 3 programming enable



Address: *ClkBBaseAddress* + 0x040

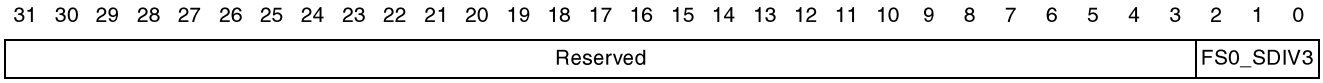
Type: R/W

Reset: 0x01

Description: Defines the PRG_EN parameter (programming enable) for the frequency synthesizer FS0 channel 3. This parameter must be set to 1 to take into account a new configuration.

0: PE3 and MD3 parameters are ignored
1: PE3 and MD3 parameters are taken into account

CKGB_FS0_SDIV3 FS0 channel 3 output clock divider



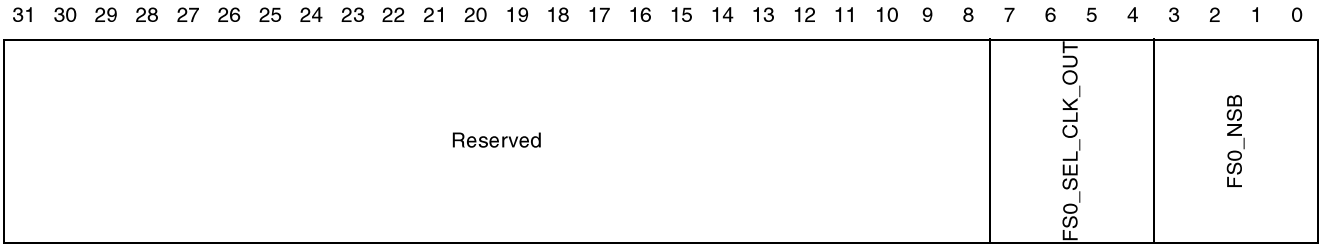
Address: *ClkBBaseAddress* + 0x044

Type: R/W

Reset: 0x02

Description: Defines the SDIV3 parameter (output divider control) for the frequency synthesizer FS0 channel 3.

CKGB_FS0_PWR_DN FS1 digital part power-down/up



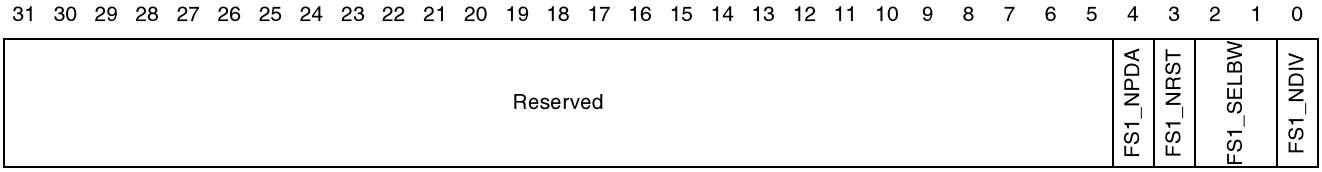
Address: *ClkBBaseAddress* + 0x58
Type: R/W
Reset: 0x77
Description: Controls the standby mode of the FS0 digital part.

[31:8] **Reserved**

[7:4] **FS0_SEL_CLK_OUT**
Must be set to 0x7

[3:0] **FS0_NSB**
Control independently the standby mode of the digital part of the 4 channels - Active low.

CKGB_FS1_CFG Global FS1 parameters



Address: *ClkBBaseAddress* + 0x5C
Type: R/W
Reset: 0x18
Description: Defines the FS1 frequency synthesizer global parameters.

[31:5] **Reserved**

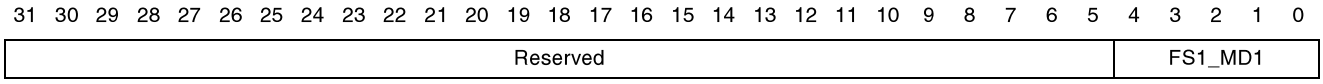
[4] **FS1_NPDA**: Analog power down mode
0: Analog power down
1: Analog power up

[3] **FS1_NRST**: Software reset
0: Reset active
1: Running

[2:1] **FS1_SELBW**: Bandwidth selection for ref clock noise reduction
00: Good reference (bandwidth = 2.4 MHz)
01: Very bad reference (bandwidth = 0.8 MHz)
10: Bad reference (bandwidth = 1.2 MHz)
11: Very good reference (bandwidth = 4 MHz)

[0] **FS1_NDIV**: Select the input frequency, if NDIV is set to
0: Ref clock frequency must be 27/30 MHz
1: Ref clock frequency must be 54/60 MHz

CKGB_FS1_MD1 FS1 channel 1 coarse selection (CLK_DISP_ID)



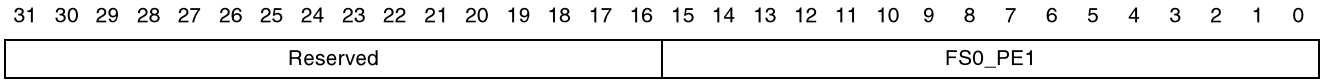
Address: *ClkBBaseAddress* + 0x060

Type: R/W

Reset: 0x09

Description: Defines the MD1 parameter (coarse selection) for the frequency synthesizer FS1 channel 1.

CKGB_FS1_PE1 FS1 channel 1 fine selection (CLK_DISP_ID)



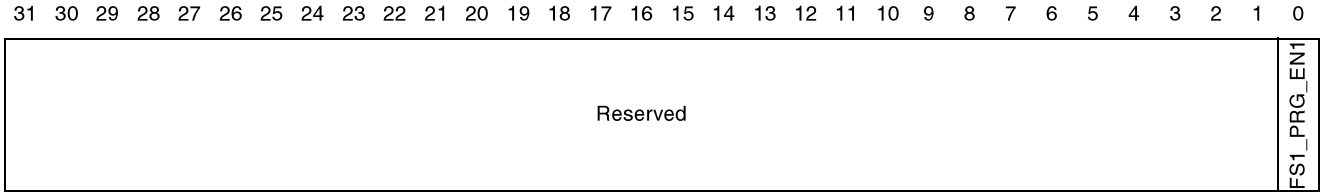
Address: *ClkBBaseAddress* + 0x064

Type: R/W

Reset: 0x1C72

Description: Defines the MD1 parameter (fine selection) for the frequency synthesizer FS1 channel 1.

CKGB_FS1_PRG_EN1 FS1 channel 1 programming enable (CLK_DISP_ID)



Address: *ClkBBaseAddress* + 0x068

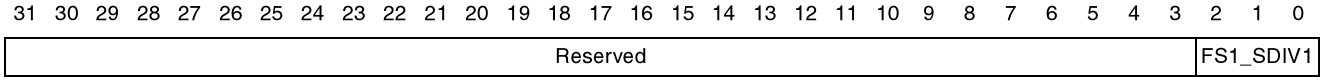
Type: R/W

Reset: 0x1

Description: Defines the PRG_EN parameter (programming enable) for the frequency synthesizer FS1 channel 1. This parameter must be set to 1 to take into account a new configuration.

0: PE1 and MD1 parameters are ignored
1: PE1 and MD1 parameters are taken into account

CKGB_FS1_SDIV1 FS1 channel 1 output clock divider (CLK_DISP_ID)



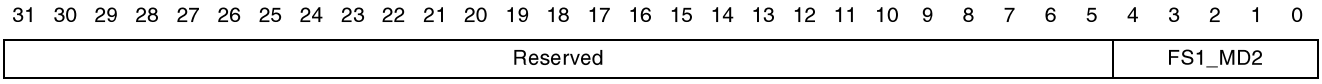
Address: *ClkBBaseAddress* + 0x06C

Type: R/W

Reset: 0x03

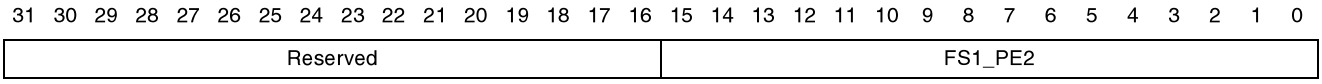
Description: Defines the SDIV1 parameter (output divider control) for the frequency synthesizer FS1 channel 1.

CKGB_FS1_MD2 FS1 channel 2 coarse selection (CLK_PIPE)



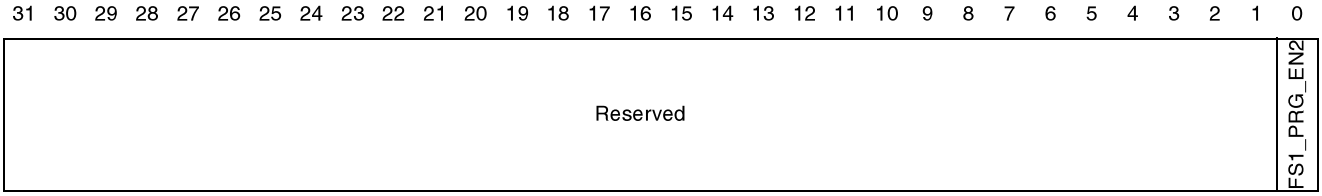
Address: *ClkBBaseAddress* + 0x070
Type: R/W
Reset: 0x19
Description: Defines the MD2 parameter (coarse selection) for the frequency synthesizer FS1 channel 2.

CKGB_FS1_PE2 FS1 channel 2 fine selection (CLK_PIPE)



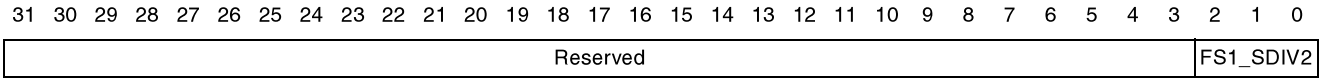
Address: *ClkBBaseAddress* + 0x074
Type: R/W
Reset: 0x3333
Description: Defines the PE2 parameter (fine selection) for the frequency synthesizer FS1 channel 2.

CKGB_FS1_PRG_EN2 FS1 channel 2 programming enable (CLK_PIPE)



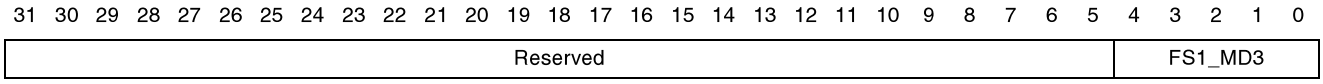
Address: *ClkBBaseAddress* + 0x078
Type: R/W
Reset: 1
Description: Defines the PRG_EN parameter (programming enable) for the frequency synthesizer FS1 channel 2. This parameter must be set to 1 to take into account a new configuration.

CKGB_FS1_SDIV2 FS1 channel 2 output clock divider (CLK_PIPE)



Address: *ClkBBaseAddress* + 0x07C
Type: R/W
Reset: 0
Description: Defines the SDIV2 parameter (output divider control) for the frequency synthesizer FS1 channel 2.

CKGB_FS1_MD3 FS1 channel 3 coarse selection



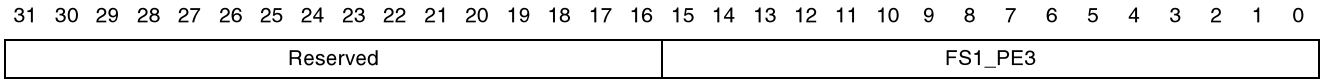
Address: *ClkBBaseAddress* + 0x080

Type: R/W

Reset: 0x11

Description: Defines the MD3 parameter (coarse selection) for the frequency synthesizer FS1 channel 3.

CKGB_FS1_PE3 FS1 channel 3 fine selection



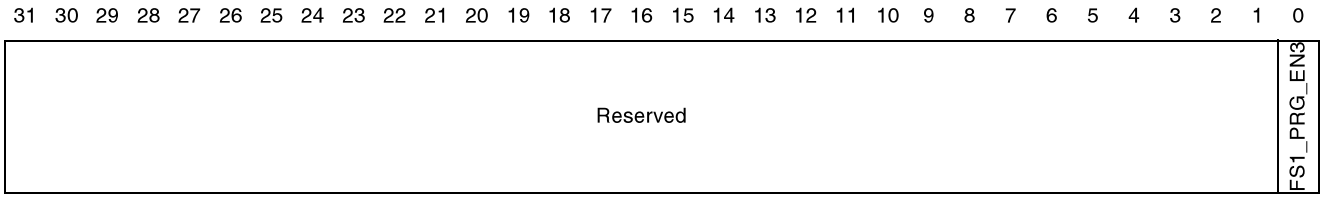
Address: *ClkBBaseAddress* + 0x084

Type: R/W

Reset: 0x1C72

Description: Defines the PE3 parameter (fine selection) for the frequency synthesizer FS1 channel 3.

CKGB_FS1_PRG_EN3 FS1 channel 3 programming enable



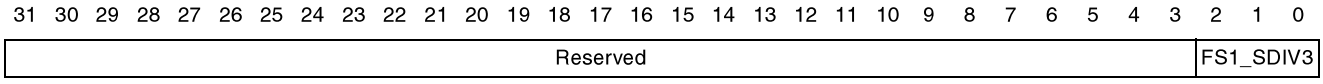
Address: *ClkBBaseAddress* + 0x088

Type: R/W

Reset: 1

Description: Defines the PRG_EN parameter (programming enable) for the frequency synthesizer FS1 channel 3. This parameter must be set to 1 to take into account a new configuration.

CKGB_FS1_SDIV3 FS1 channel 3 output clock divider



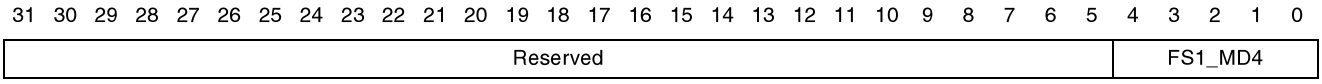
Address: *ClkBBaseAddress* + 0x08C

Type: R/W

Reset: 0x03

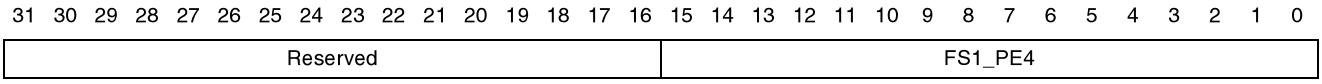
Description: Defines the SDIV3 parameter (output divider control) for the frequency synthesizer FS1 channel 3. Range: from 2 to 256.

CKGB_FS1_MD4 FS1 channel 4 coarse selection (CLK_LPC)



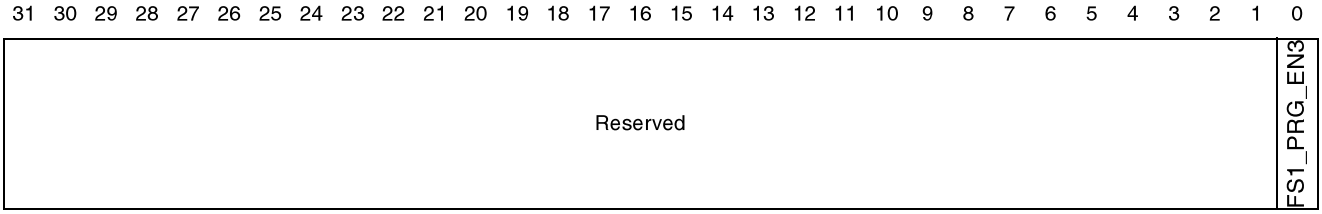
Address: *ClkBBaseAddress* + 0x090
Type: R/W
Reset: 0x13
Description: Defines the MD4 parameter (coarse selection) for the frequency synthesizer FS1 channel 4.

CKGB_FS1_PE4 FS1 channel 4 fine selection (CLK_LPC)



Address: *ClkBBaseAddress* + 0x094
Type: R/W
Reset: 0x00
Description: Defines the PE4 parameter (fine selection) for the frequency synthesizer FS1 channel 4.

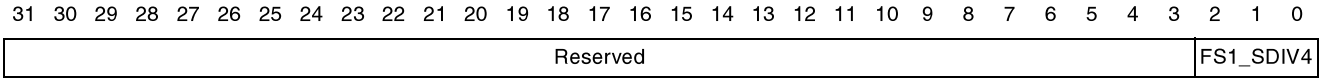
CKGB_FS1_PRG_EN4 FS1 channel 4 programming enable (CLK_LPC)



Address: *ClkBBaseAddress* + 0x098
Type: R/W
Reset: 1
Description: Defines the PRG_EN parameter (programming enable) for the frequency synthesizer FS1 channel 4. This parameter must be set to 1 to take into account a new configuration.

0: PE3 and MD3 parameters are ignored
1: PE3 and MD3 parameters are taken into account.

CKGB_FS1_SDIV4 FS1 channel 4 output clock divider (CLK_LPC)



Address: *ClkBBaseAddress* + 0x09C
Type: R/W
Reset: 2
Description: Defines the SDIV3 parameter (output divider control) for the frequency synthesizer FS1 channel 4. Range: from 2 to 256.

CKGB_FS1_PWR_DN FS1 digital part power-down/up

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												FS1_NSB			

Address: *ClkBBaseAddress* + 0x0A0

Type: R/W

Reset: 0xFF

Description: Controls stand-by mode of the FS1 digital part.

[31:4] **Reserved**
Must be set to 7.

[3:0] **FS1_NSB**
Control independently the stand-bye mode of the digital part of the four channels - Active low.

CKGB_DISP_CFG Video display clocks configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				CLK_PIX_SD_SEL		CLK_DISP_ID_SEL		CLK_656_SEL		CLK_DISP_HD_SEL		CLK_PIX_HDMI		CLK_TMDS_HDMI	

Address: *ClkBBaseAddress* + 0x0A4

Type: R/W

Reset: 0x469

Description: HD and SD video display clocks configuration.

[31:12] **Reserved**

[11:10] **CLK_PIX_SD_SEL**
00: CLK_PIX_SD = CLK_FS0_CHAN1 / 2
01: CLK_PIX_SD = CLK_FS0_CHAN1 / 4
10: CLK_PIX_SD = CLK_FS0_CHAN1 / 8
11: CLK_PIX_SD = CLK_FS0_CHAN1 / 2

[9:8] **CLK_DISP_ID_SEL**
00: CLK_DISP_ID = CLK_FS1_CHAN1 / 2
01: CLK_DISP_ID = CLK_FS1_CHAN1 / 4
10: CLK_DISP_ID = CLK_FS1_CHAN1 / 8
11: CLK_DISP_ID = CLK_FS1_CHAN1 / 2

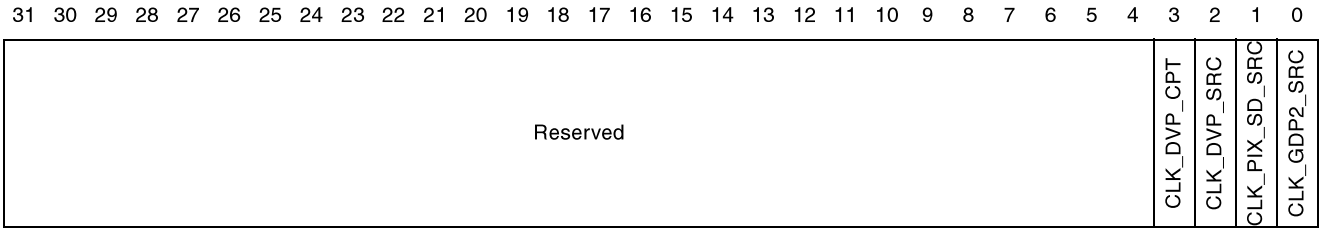
[7:6] **CLK_656_SEL**
00: CLK_656 = CLK_FS0_CHAN1 / 2
01: CLK_656 = CLK_FS0_CHAN1 / 4
10: CLK_656 = CLK_FS0_CHAN1 / 8
11: CLK_656 = CLK_FS0_CHAN1 / 2

[5:4] **CLK_DISP_HD_SEL**
00: CLK_DISP_HD = CLK_FS0_CHAN1 / 2
01: CLK_DISP_HD = CLK_FS0_CHAN1 / 4
10: CLK_DISP_HD = CLK_FS0_CHAN1 / 8
11: CLK_DISP_HD = CLK_FS0_CHAN1 / 2

[3:2] **CLK_PIX_HDMI**
00: CLK_PIX_HDMI = CLK_FS0_CHAN1 / 2
01: CLK_PIX_HDMI = CLK_FS0_CHAN1 / 4
10: CLK_PIX_HDMI = CLK_FS0_CHAN1 / 8
11: CLK_PIX_HDMI = CLK_FS0_CHAN1 / 2

[1:0] **CLK_TMDS_HDMI**
00: CLK_TMDS_HDMI = CLK_FS0_CHAN1 / 2
01: CLK_TMDS_HDMI = CLK_FS0_CHAN1 / 4
10: CLK_TMDS_HDMI = CLK_FS0_CHAN1 / 8
11: CLK_TMDS_HDMI = CLK_FS0_CHAN1 / 2

CKGB_CLK_SRC Clock source selection



Address: *ClkBBaseAddress* + 0x0A8

Type: R/W

Reset: 0x06

Description: Defines the clock source when more than one source is possible.

[31:4] **Reserved**

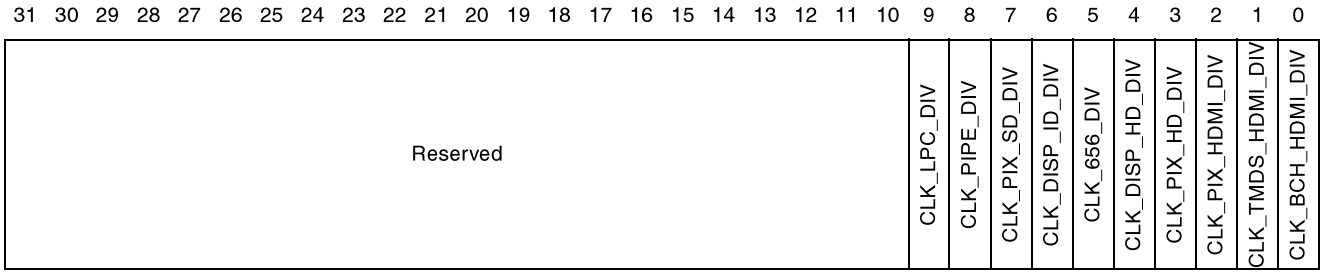
[3] **CLK_DVP_CPT**: CLK_DVP capture
0: CLK_DVP sourced from VIDINCLK input pin
1: CLK_DVP sourced from frequency synthesizers

[2] **CLK_DVP_SRC**
0: CLK_DVP sourced from FS0
1: CLK_DVP sourced from FS1
Note: CLK_DVP sourced from frequency synthesizers only if CLK_DVP_CPT=1

[1] **CLK_PIX_SD_SRC**
0: CLK_PIX_SD sourced from FS0
1: CLK_PIX_SD sourced from FS1

[0] **CLK_GDP2_SRC**
0: CLK_GDP2 sourced from FS0
1: CLK_GDP2 sourced from FS1

CKGB_CLK_DIV Individual clocks division



Address: *ClkBBaseAddress* + 0xAC

Type: R/W

Reset: 0

Description: Run clocks generated from clock generator B at nominal or reduced frequency, allowing reduced power consumption. The clock affected is shown by the name of the bitfield, for example CLK_LPC_DIV controls CLK_LPC.

0: Run at nominal frequency
1: Run at 1/1024 frequency

[31:10] **Reserved**

[9] **CLK_LPC_DIV**

[8] **CLK_PIPE_DIV**

[7] **CLK_PIX_SD_DIV**

[6] **CLK_DISP_ID_DIV**

[5] **CLK_656_DIV**

[4] **CLK_DISP_HD_DIV**

[3] **CLK_PIX_HD_DIV**

[2] **CLK_PIX_HDMI_DIV**

[1] **CLK_TMDS_HDMI_DIV**

[0] **CLK_BCH_HDMI_DIV**

CKGB_CLK_EN Individual clocks enable

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																		CLK_LPC_EN	CLK_TTXT_EN	CLK_PIPE_EN	CLK_PIX_HDMI_EN	CLK_PIX_SD_EN	CLK_DISP_ID_EN	CLK_GDP2_EN	CLK_656_EN	CLK_TMDS_HDMI_EN	CLK_DISP_HD_EN	CLK_PIX_HD_EN	CLK_BCH_HDMI_EN	CLK_DSS_EN	CLK_DAA_EN

Address: *ClkBBaseAddress* + 0x0B0

Type: R/W

Reset: 0x2FFF

Description: Stop or enable clocks generated from clock generator B. The clock affected is shown by the name of the bitfield, for example CLK_LPC_EN controls CLK_LPC.

0: Stop
1: Enable

[31:14] **Reserved**

[13] **CLK_LPC_EN**

[12] **CLK_TTXT_EN**

[11] **CLK_PIPE_EN**

[10] **CLK_PIX_HDMI_EN**

[9] **CLK_PIX_SD_EN**

[8] **CLK_DISP_ID_EN**

[7] **CLK_GDP2_EN**

[6] **CLK_656_EN**

[5] **CLK_TMDS_HDMI_EN**

[4] **CLK_DISP_HD_EN**

[3] **CLK_PIX_HD_EN**

[2] **CLK_BCH_HDMI_EN**

[1] **CLK_DSS_EN**

[0] **CLK_DAA_EN**

CKGB_CLKOUT_SEL Clocks observation selection

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								CLKOUT_SEL							

Address: *ClkBBaseAddress* + 0x0B4

Type: R/W

Reset: 0

Description: Selects which clock of clockgen B to be routed to the PIO5[2] (SYSCLKOUTB) pin.

Table 77: PIO5[2] pin source

CLKOUT_SEL	SYSCLKOUTB
0000 0000	CLK_BCH_HDMI
0000 0001	CLK_TMDS_HDMI
0000 0010	CLK_PIX_HDMI
0000 0011	CLK_PIX_HD
0000 0100	CLK_DISP_HD
0000 0101	CLK_656
0000 0110	CLK_GDP2
0000 0111	CLK_DISP_ID
0000 1000	CLK_PIX_SD
0000 1001	CLK_DSS
0000 1010	CLK_DAA
0000 1011	CLK_PIPE
0000 1100	CLK_TTXT
0000 1101	CLK_LPC
0000 1110	CLK_DVP
1011 1100	CLK_PP
1100 1100	CLK_IC_150
All others	Reserved

CKGB_REFCLK_SEL Reference clock source selection

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															REFCLK_SEL

Address: *ClkBBaseAddress* + 0x0B8

Type: R/W

Reset: 0

Description: Allows selection of clockgen B reference clock. this can be either the internal 30 MHz clock used by the SATA and USB interfaces or an external clock connected to the SYSBCLKINALT pin.

0: Internal 30 MHz clock
1: External clock

17 Reset

17.1 Overview

The different reset sources are:

- The power-on reset signal applied to the NOTRESETIN pad
- The watchdog reset signal generated by the ST40 internal watchdog-timer (WDT)
- The security violation reset
- The UDI reset command received via the ST40 debug port
- The software reset applied to the ST231 CPUs via the SYS_CFG27 and SYS_CFG29 configuration registers.

A reset output pin NOTWDOGRSTOUT is provided to control the reset of external devices. The length of this reset signal can be controlled with the mode pin EMIADDR[14].

Boot and reset registers are described in Chapter 21: *System configuration registers on page 171*. See also Chapter 20: *Boot modes on page 169*.

17.2 Power-on reset

The complete reset sequence is executed only during a “power-on-reset” sequence (cold reset). In this sequence, everything is reset including the clock generators and the values captured on the mode pins during the reset phase.

17.3 System reset

When the reset source is the security checker, the watchdog timer or the UDI, then a “system reset” sequence is executed (warm reset). In that sequence, everything is reset except the clock generators, the antifuses and some of the system configuration registers. The mode pins values sampled during the power-on-reset are kept unchanged.

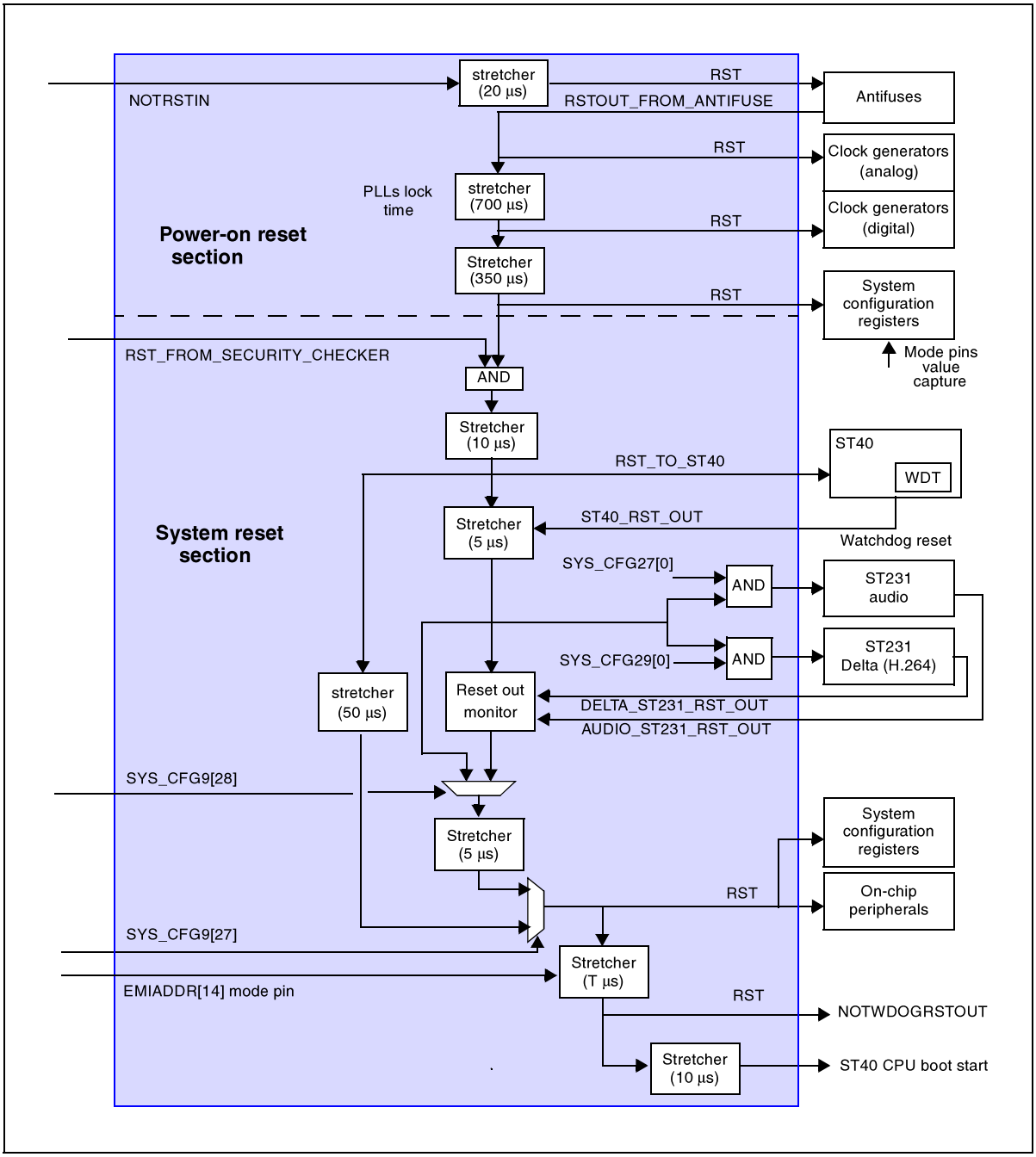
17.4 Reset sequence

The reset sequence controlled by the reset generator is as follows:

1. The clock generators A and B are reset. When the PLLs are locked and the clock generators are reset then the reset propagation continues.
2. The ST40 CPU is reset. When the ST40 internal reset sequence is ended then the reset propagation continues.
3. The audio and Delta (H.264) ST231s are reset. When the ST231s’ reset sequences are ended then the reset propagation continues. When reset, the audio and Delta ST231 boot, but their access to the memory is halted. The configuration registers SYS_CFG26[0] and SYS_CFG28[0] must be set by the ST40 to authorize memory accesses (see Chapter 20: *Boot modes on page 169*).
4. All on-chip peripherals are reset. The reset propagation continues.
5. The reset signal on the NOTWDOGRSTOUT output pin is de-asserted after a delay defined by the mode pin value EMIADDR[14].
6. The ST40 boots and starts to execute its code.

The reset sequence controlled by the reset generator takes into account the antifuse reset timing sequence, some optional reset configuration (short or long reset) and the internal reset sequences of the ST40 and ST231s CPUs. This is shown in Figure 55.

Figure 55: Reset generator block diagram



17.5 CPUs reset and reset out

17.5.1 Power-on reset

Both the ST40 and ST231s are reset when a reset signal is applied to the NOTRESETIN input pin. In that case, the reset signal is propagated and all the CPUs and internal peripherals are reset in sequence.

17.5.2 ST231 software reset

The audio and Delta ST231 CPUs can be reset by the ST40 using the configuration registers SYS_CFG27[0] and SYS_CFG29[0]. Setting the bit 0 to 1 produces a reset to the ST231. Resetting the bit 0 to 0 releases the software reset.

17.5.3 ST231 reset out bypass

When reset, the ST231 starts an internal reset sequence. It indicates that it has ended this sequence by asserting a reset out signal. By default, this reset out signal is used to propagate the reset to all the peripherals (internal and external).

Before applying a software reset to the ST231, this reset out signal must be bypassed, otherwise not only the ST231 will be reset but all the peripherals. The configuration bit SYS_CFG9.CPU_RST_OUT_BYPASS1 (bit 28) is provided to bypass both the Delta and audio ST231 reset out signals. This must be used when the default ST231 boot address is changed and a reset must be applied (see Chapter 20: *Boot modes on page 169*).

17.6 ST40 watchdog timeout reset

The ST40 includes a watchdog timer (WDT) that can generate a timeout event. In case of timeout, a system reset is generated.

Using the watchdog timer mode:

1. Set the WT/IT bit in the WTCSR (watchdog timer control/status) register to 1 to set the timer in watchdog mode, select the type of reset with the RSTS bit, and the count clock with bits CKS2-CKS0, and set the initial value in the WTCNT counter.
2. When the TME bit (timer enable) in the WTCSR register is set to 1, the count starts in watchdog timer mode.
3. During operation in watchdog timer mode, write 0x00 to the counter periodically so that it does not overflow.
4. When the counter overflows, the WDT sets the WOVF flag in the WTCSR register to 1, and generates a reset of the type specified by the RSTS bit. The counter then continues counting.

For more details on the ST40 watchdog timer, refer to the ST40 documentation cited in Chapter 4: *CPUs on page 37*.

17.7 NOTWDOGRSTOUT signal length

The NOTWDOGRSTOUT signal length can be either around 1.2 ms when the mode pin EMIADDR[14] is set to 0, or around 200 ms when the mode pin EMIADDR[14] is set to 1.

18 Low-power modes

18.1 Overview

Power saving can be achieved by halting the ST40 CPU and stopping or reducing the clock frequencies. The ST231 CPU clocks can either be stopped or kept running at a low frequency. In addition, a number of functional blocks can be disabled.

Reducing the clocks' frequency dramatically reduces the power consumption, and still enables the execution of some software.

When the ST40 is in one of the low-power modes ("sleep" or "standby"), it can be woken up either by a reset, an NMI interrupt, an ST40 peripheral interrupt or an external interrupt.

Before entering the low-power modes, the DDRs can be set in self-refresh mode via a special sequence of the memory controller.

The code to be executed by the CPU when it is awoken must reside in EMI if the DDRs are in self-refresh mode. In that case, the EMI clock must be kept running at a low frequency.

The different functional units involved in the low-power feature are:

- the ST40, which can be halted by executing the SLEEP instruction,
- the clock generators A, B and C, which can be configured by software to generate low-frequency clocks. They can also automatically enter the low-power mode when they detect an event from the low-power controller (LPC) and automatically exit from low-power mode when a wake-up interrupt is detected by the ILC. In low-power mode, the clocks are automatically divided by 1024. The unnecessary clocks can be stopped by configuration registers,
- the IRB/UHF Rx processor, which can detect an activity on the IRB/UHF inputs (PIO3[3] and PIO3[4]) and can generate a wake-up interrupt to the ST40 and exit the clock generators from their low-power mode,
- the ILC, which must be configured to map the ST40 interrupts IRL(3-0) to 4 of the following external interrupts: SYSITRQ(3-0), UHF_WAKEUP (PIO3[4]), IRDA_WAKEUP (PIO3[3]). These signals are connected to the ILC (EXT_INT[5-0] input pins in Figure 56 below) and can be used as a wake-up interrupt for the ST40 (see Table 78 below).
- the low-power controller (LPC), which includes a 40-bit low-power alarm counter (LPA). The LPC is used to put the clock generators in low-power mode. The LPA timer is used to exit from low-power after a user-defined delay. The LPA timer is clocked by the CLK_LPC clock defined in clock generator B.

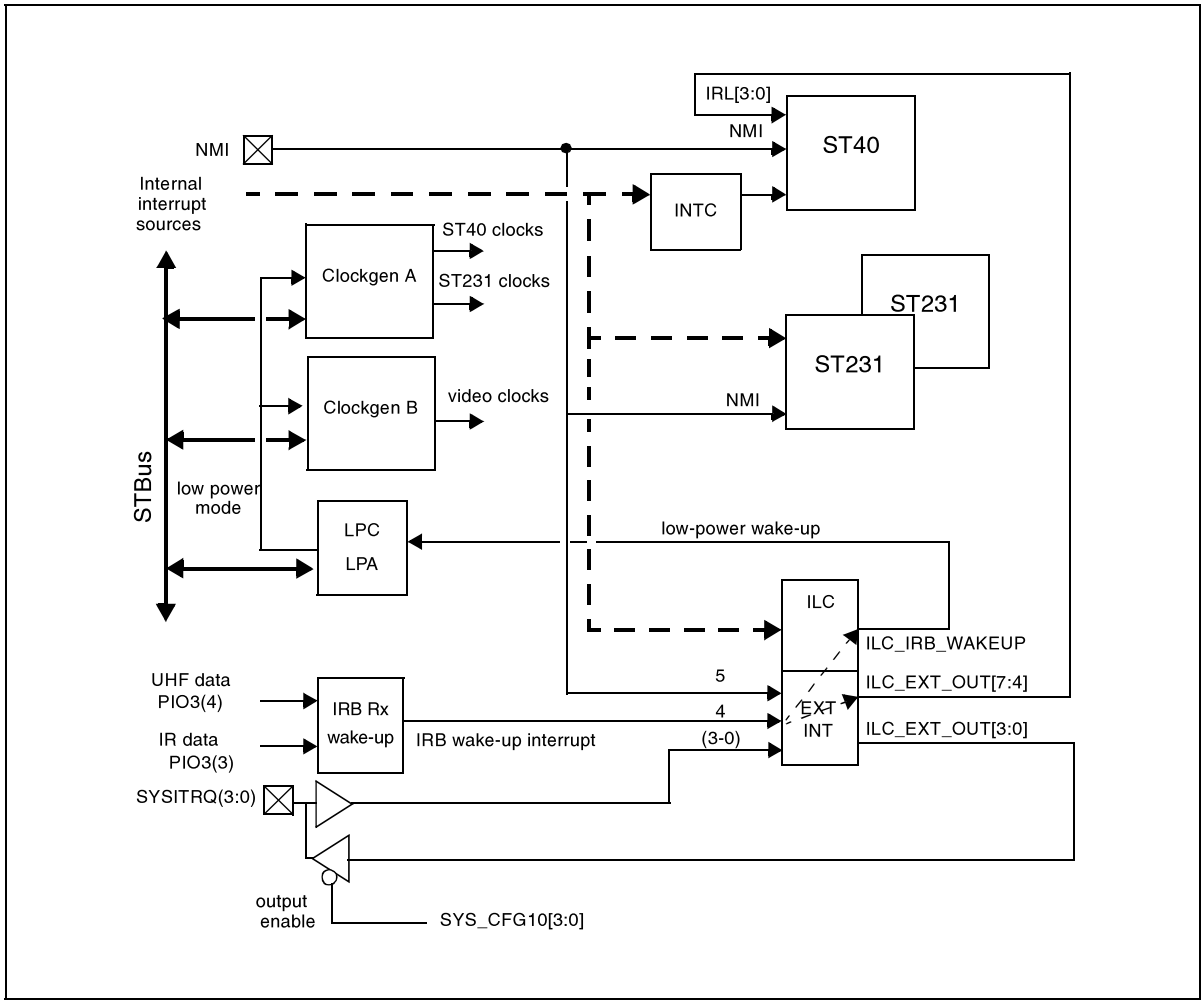
The ILC wake-up interrupt sources are described in Table 78 below.

Table 78: ILC external wake-up interrupt

ILC external interrupt input	Interrupt source	Description
EXT_INT(0)	SYSITRQ(0)	External interrupt input
EXT_INT(1)	SYSITRQ(1)	External interrupt input
EXT_INT(2)	SYSITRQ(2)	External interrupt input
EXT_INT(3)	SYSITRQ(3)	External interrupt input
EXT_INT(4)	IRB wake-up	Wake-up interrupt from the IRB Rx
EXT_INT(5)	NMI	Non-maskable interrupt

Figure 56 describes the connections between those units.

Figure 56: STx7100 low-power diagram



18.2 ST40 low-power modes

The ST40 provides two low-power modes which halt the CPU:

- sleep,
- standby.

When it is in sleep mode, the ST40 is halted, its registers are held, but the ST40 peripherals continue to operate.

When it is in standby mode, the ST40 is halted, its registers are held, but the ST40 peripherals are stopped.

Transition to sleep and standby modes

If a SLEEP instruction is executed with bit STDBY of register CPG.STBCR. set to 0, then the ST40 switches from the program execution state to sleep mode (See Chapter 4: *CPUs on page 37*). If the SLEEP instruction is executed with bit STDBY set to 1, then the ST40 enters the standby mode.

Exiting from sleep and standby modes

A reset, or a NMI interrupt or an external interrupt IRL(3-0) can be used to exit from both sleep and standby modes.

18.3 Reducing or/and stopping the clocks

Most of the clocks generated by the clockgen A and clockgen B can be put in low-power mode (divided by 1024). This can be achieved either by programming the clock generator configuration registers or automatically using the LPA (low power alarm) timer of the LPC (low power controller) module.

Using the clock generators configuration registers

See also Chapter 15: *Clocks on page 120* and Chapter 16: *Clock registers on page 134*.

All clocks can be programmed through configuration registers to be slowed by a factor of 1024 except the following:

- ST40 clocks (CLK_ST40, CLK_ST40_IC, CLK_ST40_PER),
- MPEG2 decoder clock,
- FDMA clock,
- interconnect and EMI clocks (CLK_IC, CLK_IC_DIV2, CLK_EMI),
- Delta decoder processing clock (CLK_PP),
- SmartCard, DAA and RTC clocks (CLK_DSS, CLK_DAA, CLK_RTC).

Before entering a low-power mode, these clocks can be redefined with a lower frequency or stopped.

To exit from low-power mode, the clock generator configuration registers must be reprogrammed.

Using the low power alarm

A global power-down command can be issued by the LPC controller. Bit 0 of register LPC_LPA_STRT must be set to 1 to enter the low-power mode.

First, a value must be written to the LPC_LPA registers to initialize the LPA timer. When the LPA counter reaches 0 then a global power-down event is generated that automatically exits the clock generators from the low-power mode. The clock nominal frequencies are then restored.

The duration of the LPA countdown can range from a few milliseconds to several hundred days.

Programming the minimum frequency for the ST40, EMI and interconnect clocks

To minimize power consumption, the ST40, interconnect and EMI clocks can be programmed to their smallest value.

This value is obtained when clockgen A PLL0 and PLL1 are set up for 6.25 MHz (MDIV=27, NDIV=100, PDIV=32). Hence, the ST40 clocks become 3.125 MHz, 1.5625 MHz and 781 kHz. The interconnect clocks become 3.125 MHz and 1.5625 MHz and the EMI clock becomes 781 kHz.

18.4 ILC interrupt controller: wake-up interrupt

The ILC is used to configure the wake-up interrupt. The registers ILC_WAKEUP_EN and ILC_WAKEUP_ACTIVE_LEVEL must be configured to define which interrupt will be used as a wake-up interrupt and its active polarity.

The ILC must also be configured to map the four ST40 external interrupts IRL(3-0) to the ILC inputs EXT_INT(5-0). For this purpose the registers ILC_SET_EN2, ILC_EXT_MODEn and ILC_EXT_PRIORITYn must be set accordingly. This interrupt is then used as a wake-up interrupt to exit the ST40 from its sleep or standby mode.

For more details on ILC programming, see Chapter 22: *Interrupt system on page 196*.

18.5 DDR self-refresh

To put the system LMI DDR in self-refresh mode, the CPU must set SYS_CFG11.LMI_SYS_PWRD_REQ (bit 28, DDR power-down request) to 1. For the video LMI DDRs, SYS_CFG11.LMI_VID_PWR_DN_REQ (bit 30) must be set to 1.

This write operation activates the power-down protocol of the memory controller (LMI core). The memory controller completes all the outstanding operations and then puts the DDRs in self-refresh mode. When the system DDRs are in self-refresh mode, SYS_STA12.LMI_SYS_PWRD_ACK[28] (system DDR power-down acknowledge) is set. When the video DDRs are in self-refresh mode, SYS_STA13.LMI_VID_PWRD_ACK[28] is set.

As soon as this acknowledge is received, the LMI clocks (in clockgen A) can be switched off or slowed down.

After exiting low-power mode, the DDR padlogic DLLs and the memory controller must be reset using SYS_CFG11.LMI_SYS_RST_N[6] and SYS_CFG11.LMI_VID_RST_N[15].

18.6 Low-power mode sequence

Entering the low-power modes

1. Configure the ILC to determine which interrupt will be used to exit the ST40 from sleep or standby mode. This interrupt (IRB, NMI or external) is routed to the ST40. The same interrupt must be declared as a wake-up interrupt for the LPC controller.

   Example: use EXT_INT(4) as a wake-up interrupt (corresponds to IRB wake-up)

   set bit 4 of ILC_WAKEUP_EN to define EXT_INT(4) as a wake-up interrupt

   set bit 4 of ILC_WAKEUP_ACTIVE_LEVEL to define the active level of the interrupt

   set bit 4 of ILC_SET_EN2 to enable EXT_INT(4)

   write 0x01 in register ILC_EXT_MODE4 to define a high-level interrupt

   write 0x8004 in register ILC_EXT_PRIORITY4 to map the EXT_INT(4) interrupt to the ST40 IRL(0)
2. Put the DDRs in self-refresh mode
3. Configure the clockgen A and B to stop the unnecessary clocks and to slow-down the ST40, EMI and interconnect clocks.
4. Configure the LPA counter time-out by writing in LPC_LPA_LS and LPC_LPA_MS
5. Enter the clock generators low-power mode by setting LPC_LPA_START.STRT.
6. Execute the SLEEP instruction (the ST40 will be either in sleep or standby mode depending on the value of CPG.STBCR).

Exiting the low-power modes

The STx7100 exits from low-power mode on either of the following events:

- the LPA counter reaches 0,
- a wake-up interrupt has occurred (reset, NMI, external, IRB wake-up).

After exiting a low-power mode, the nominal clock frequencies are restored. The clocks that were stopped can be restarted.

If the DDRs are in self-refresh mode then a software reset to the DDR padlogic and memory controller must be applied.

LPC clock frequency

In standby mode, the LPC clock frequency must be less or equal to the RTC clock frequency.

19 Low power registers

Register addresses are provided as *LPC_LPABaseAddress* + offset.

The *LPC_LPABaseAddress* is:

0x1800 8000.

Table 79: Low power alarm register summary

Register	Description	Offset	Type
LPC_LPA_LS	LPA - low power alarm timer (LSB)	0x0410	R/W
LPC_LPA_LS	LPA - low power alarm timer (MSB)	0x0414	R/W
LPC_LPA_START	LPA - low power alarm timer start	0x0418	R/W

LPC_LPA_LS Low power alarm timer low value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPA_TMR[31:0]																															

Address: *LPC_LPABaseAddress* + 0x0410

Type: R/W

Reset: 0

Description: Defines the four least significant bytes of the low power alarm counter.

LPC_LPA_MS Low power alarm timer high value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								LPA_TMR[39:32]							

Address: *LPC_LPABaseAddress* + 0x0414

Type: R/W

Reset: 0

Description: Defines the most significant byte of the low power alarm counter.

LPC_LPA_START Low power alarm timer start

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															START

Address: *LPC_LPABaseAddress* + 0x0418

Type: R/W

Reset: 0

Description: Setting the bit 0 to 1 starts the low power alarm counter. The counter starts to count down from the value defined in LPC_LPA_MS and LPC_LPA_LS.

20 Boot modes

The STx7100 has three boot modes, controllable by two external pins: BOOTMODE[1:0]. These pins are strobed at the end of the reset period (power-on or watch-dog resets). The boot code must be stored in flash memory attached to the EMI bus.

The boot system is closely connected with reset; see Chapter 17: *Reset on page 161*. Boot and reset registers are described in Chapter 21: *System configuration registers on page 171*.

- **ST40 mode** (Default): This is the standard mode, in which the ST40 boots first from EMI. The Delta and audio ST231 boot requests are both halted by the interconnect. It is up to the ST40 software to control the boot sequence of the two ST231. The boot address of the ST231s must be defined in the system configuration registers before the boot request is released by the ST40.
- **Delta (H.264) ST231 mode**: The ST40 boot request is halted by the interconnect, but the boot request from the Delta ST231 is released, allowing the Delta ST231 to boot from EMI. In this mode, the Delta ST231 uses the default boot address (0x0 0000). This mode may be useful for low-level software debugging; in this mode, the ST40 is not expected to boot.
- **Audio ST231 mode**: The ST40 boot request is halted by the interconnect, but the boot request from the audio ST231 is released, allowing the audio ST231 to boot from EMI. In this mode, the audio ST231 uses the default boot address (0x0 0000). This mode may be useful for low-level software debugging; in this mode the ST40 is not expected to boot.

For security purpose, an antifuse can be set to disable the Delta and audio ST231 modes.

Table 80: Boot mode selection

BOOTMODE pins	Boot mode
00	**Default**: ST40 boots first. Delta and audio ST231 boot sequences are controlled by the ST40.
01	**Delta ST231**: ST40 boot is halted. Delta ST231 boots first and controls the ST40 and audio ST231 boot sequences.
10	**Audio ST231**: ST40 boot is halted. Audio ST231 boots first and controls the ST40 and Delta ST231 boot sequences.

20.1 Default mode

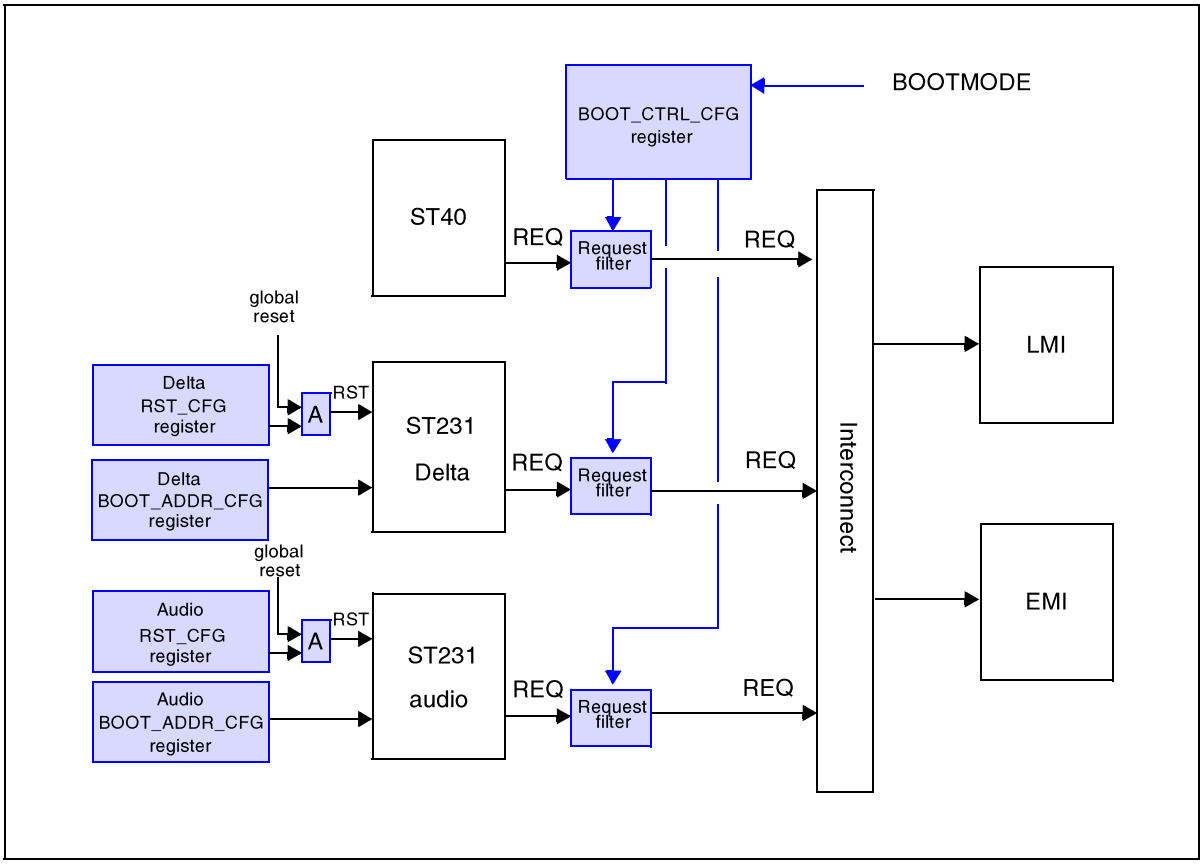
In the default boot mode, the requests of the two ST231s are filtered and halted. The ST40 boots from EMI and typically goes through the following sequence for each ST231:

1. Writes the boot code of the ST231 in EMI or LMI.
2. Updates the boot address configuration register of the ST231.
3. Resets the ST231 with the RST_CFG register.
4. Releases the request filter of the ST231 with the BOOT_CTRL_CFG register.
5. Releases the reset of the ST231.

The ST231 then executes its boot sequence.

The operation is identical for both Delta and audio ST231s.

Figure 57: Boot control block diagram



20.2 Delta ST231 mode

In this mode, the requests of the ST40 and audio ST231 are filtered and halted. The Delta ST231 boots using the default value of its boot control configuration register, which points to the EMI bottom address.

The Delta ST231 controls the boot sequence of the audio ST231 as described above.

The ST40 does not boot.

20.3 Audio ST231 mode

In this mode, the requests of the ST40 and Delta ST231 are filtered and halted. The audio ST231 boots using the default value of its boot control configuration register, which points to the EMI base address.

The audio ST231 controls the boot sequence of the Delta ST231 as described above.

The ST40 does not boot.

21 System configuration registers

21.1 Overview

The system configuration unit includes a number of configuration and status registers.

The **status registers** report the state of the following blocks:

- device identifier,
- USB and SATA,
- mode pins captured values,
- system and video LMI Padlogic.

The **configuration registers** allow the setup of the following blocks:

- transport subsystem,
- NRSSA,
- USB,
- EMI bridge,
- SATA,
- comms,
- ST40 boot,
- reset generator,
- interrupt pads direction,
- video and system LMI padlogic,
- audio ST231 boot and reset,
- Delta (H.264) ST231 boot and reset,
- SATA and USB software JTAG.

21.2 Summary

Register addresses are provided as *SysConfigBaseAddress* + offset.

The *SysConfigBaseAddress* is:

0x1900 1000

Table 81: System configuration registers summary

Name	Function	Offset	Type
Device identity			
DEVICE_ID	Device identifier	0x000	RO
EXTRA_DEVICE_ID	Extra device identifier	0x004	
Status			
SYS_STA0	USB2/SATA status	0x008	RO
SYS_STA1	Mode pin status captured during power-on-reset	0x00C	
SYS_STA2 - 11	Reserved	0x010 - 0x034	
SYS_STA12	System LMI padlogic status	0x038	
SYS_STA13	Video LMI padlogic status	0x03C	
SYS_STA14	Reserved	0x040	
Configuration			
SYS_CFG0	Transport configuration	0x100	R/W
SYS_CFG1	NRSSA configuration	0x104	
SYS_CFG2	USB configuration	0x108	
SYS_CFG3	Video DACs and HDMI configuration	0x10C	
SYS_CFG4	EMI bridge configuration	0x110	Mixed
SYS_CFG5	Reserved	0x114	-
SYS_CFG6	SATA configuration	0x118	R/W
SYS_CFG7	COMMs configuration	0x11C	
SYS_CFG8	ST40 boot control	0x120	
SYS_CFG9	Reset generator, EMI configuration	0x124	
SYS_CFG10	SYSITRQ pads configuration	0x128	
SYS_CFG11	LMI general configuration	0x12C	
SYS_CFG12	System LMI padlogic configuration	0x130	
SYS_CFG13	Video LMI padlogic configuration	0x134	
SYS_CFG14	System LMI padlogic DLL1 control	0x138	
SYS_CFG15	System LMI padlogic DLL2 control	0x13C	
SYS_CFG16 - 19	Reserved	0x140 - 0x14C	-
SYS_CFG20	Video LMI padlogic DLL1 control	0x150	R/W
SYS_CFG21	Video LMI padlogic DLL2 control	0x154	
SYS_CFG22 - 25	Reserved	0x158 - 0x164	-
SYS_CFG26	Audio ST231 boot control	0x168	R/W
SYS_CFG27	Audio ST231 reset control	0x16C	
SYS_CFG28	Delta ST231 boot control	0x170	
SYS_CFG29	Delta ST231 reset control	0x174	
SYS_CFG30 - 32	Reserved	0x178 - 0x180	-
SYS_CFG33	USB and SATA software JTAG configuration	0x184	R/W

21.3 Device identity

DEVICE_ID JTAG device ID

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERSION				GROUP_ID						DEVICE_ID										MANUFACTURER_ID											JB

Address: *SysConfigBaseAddress* + 0x000
Type: RO
Reset: 0x0D42 4041
Description:

[31:28] **VERSION**: 0000
[27:22] **GROUP_ID**: 11 0101
[21:12] **DEVICE_ID**: 00 0010 0100
[11:1] **MANUFACTURER_ID**: 000 0010 0000
[0] **JB**: JTAG bit: 1

EXTRA_DEVICE_ID Extra device ID

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIP_ID																															

Address: *SysConfigBaseAddress* + 0x004
Type: RO
Reset:
Description:

21.4 System status

SYS_STA0 System status 0 (USB & SATA JTAG, USB PLL)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										TDO_EN_SATA	TDO_SATA	TDO_EN_USB	TDO_USB	BIST_OK	RB_1440

Address: *SysConfigBaseAddress* + 0x008

Type: RO

Reset: 0

Description:

[31:6] **Reserved**

[5] **TDO_EN_SATA**
1: The SATA PHY TAP controller is shifting out

[4] **TDO_SATA**: SATA PHY TDO signal

[3] **TDO_EN_USB**
1: The USB PHY TAP controller is shifting out

[2] **TDO_USB**: USB2 PHY TDO signal

[1] **BIST_OK**: USB PHY bist status
1: No errors detected

[0] **RB_1440**: USB2 PHY PLL state
1: The PLL is locked

SYS_STA1 System status 1 (mode pins values)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																	MODE														

Address: *SysConfigBaseAddress* + 0x00C

Type: RO

Reset: Not applicable

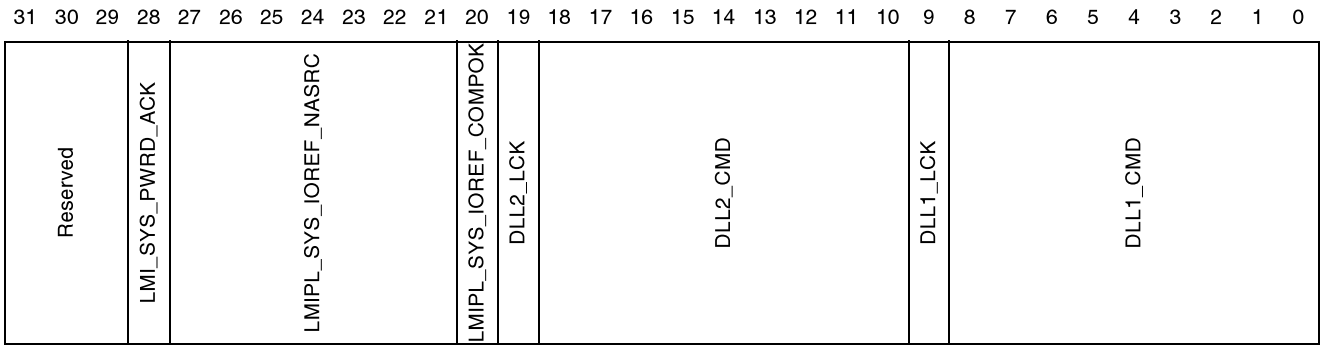
Description: Indicates the mode pins values captured during the reset phase.

[31:15] **Reserved**

[14:0] **MODE**: Values of the mode pins captured during the power-on-reset phase

		Output
[14]	Reserved	-
[13]	Short or long reset signal	Reset generator
[12:11]	Boot mode selection: 0: ST40 boot others: Reserved	System configuration
[10]	Master/slave mode	EMI subsystem
[9:8]	EMI Banks port size at boot	EMI subsystem
[7:6]	TAPmux bypass select	Reserved
[5:4]	Reset bypasses (CPU_RST_OUT_BYPASS[1:0])	Reset generator
[3:2]	PLL1 startup configuration	Clock generator A
[1:0]	PLL0 startup configuration	Clock generator A

SYS_STA12 System status 12: LMI padlogic



Address: *SysConfigBaseAddress* + 0x038

Type: RO

Reset: From padlogic

Description: Returns the status of the system LMI padlogic DLL.

[31:29] **Reserved**

[28] **LMI_SYS_PWRD_ACK**: System LMI power-down acknowledge
1 LMI is in power-down mode.
Reset:0

[27:21] **LMIPL_SYS_IOREF_NASRC**: Compensation code

[20] **LMIPL_SYS_IOREF_COMPOK**
High only in normal mode when a new measured code is available on the ASRC lines.

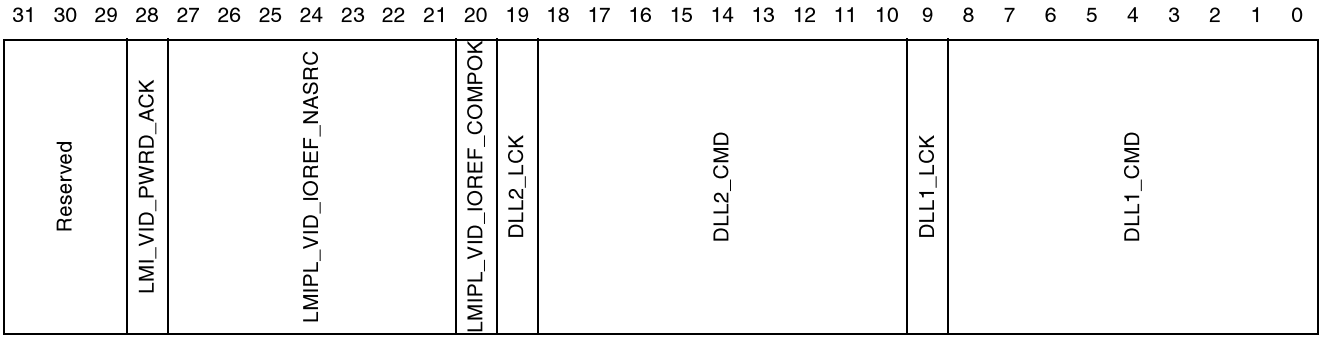
[19] **DLL2_LCK**: DLL2 lock value

[18:10] **DLL2_CMD**: DLL2 command
Reports the command currently being generated by DLL2.

[9] **DLL1_LCK**: DLL1 lock value

[8:0] **DLL1_CMD**: DLL1 command
Reports the command currently being generated by DLL1.

SYS_STA13 System status 13: video LMI padlogic



Address: *SysConfigBaseAddress* + 0x3C

Type: RO

Reset: From padlogic

Description: Returns the state of the video LMI padlogic DLL.

[31:29] **Reserved**

[28] **LMI_VID_PWRD_ACK**: Video LMI power-down acknowledge
1: LMI is in power-down mode.
Reset:0

[27:21] **LMIPL_VID_IOREF_NASRC**: Compensation code

[20] **LMIPL_VID_IOREF_COMPOK**
High only in normal mode when a new measured code is available on the ASRC lines.

[19] **DLL2_LCK**: DLL2 lock value

[18:10] **DLL2_CMD**: DLL2 command
Reports the command currently being generated by DLL2.

[9] **DLL1_LCK**: DLL1 lock value

[8:0] **DLL1_CMD**: DLL1 command
Reports the command currently being generated by DLL1.

21.5 Configuration

SYS_CFG0 System configuration 0: TS merger

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																													CFG_TS0_TS1_SEL	INPUT_SEL_MUX	BYPASS_TS

Address: *SysConfigBaseAddress* + 0x100

Type: R/W

Reset: 0

Description: Defines the transport stream merger (TSMerger) inputs configuration.

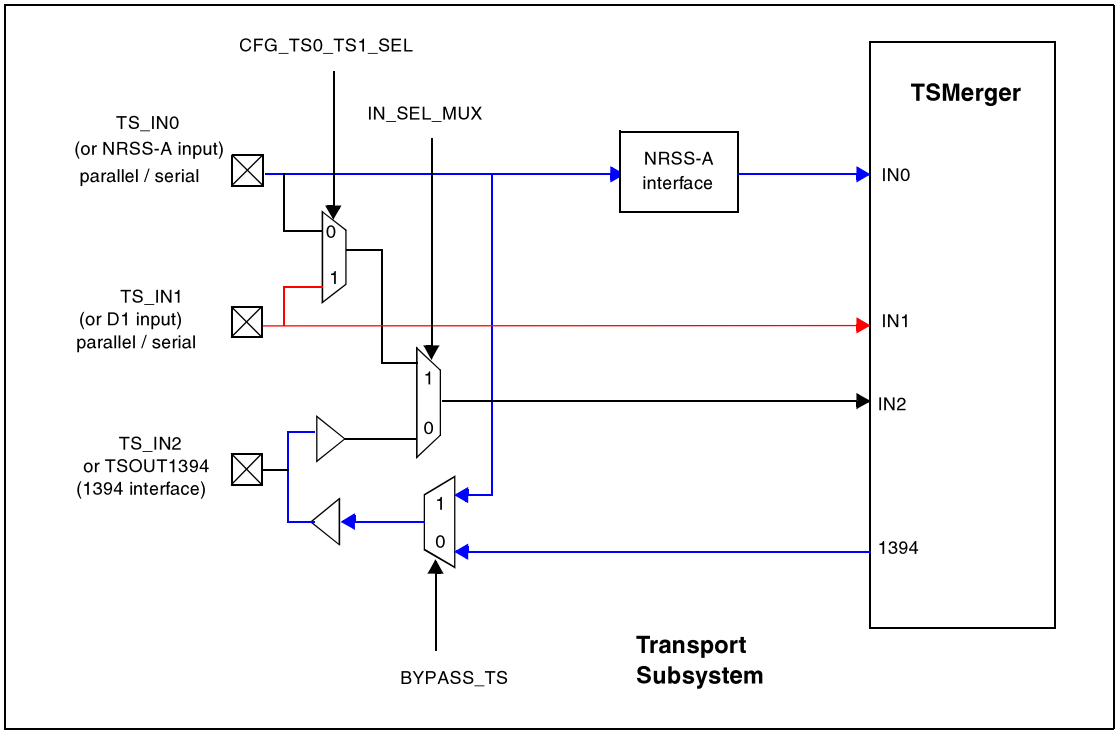
[31:] **Reserved**

[2] **CFG_TS0_TS1_SEL**: Configure TS0 TS1 select
0: TSIN0 routed to TSIN2
1: TSIN1 routed to TSIN2

[1] **IN_SEL_MUX**: Input select multiplex
0: TSMerger TSIN2 receives TSIN2
1: TSMerger TSIN2 receives TSIN0 or TSIN1 depending on CFG_TS0_TS1_SEL

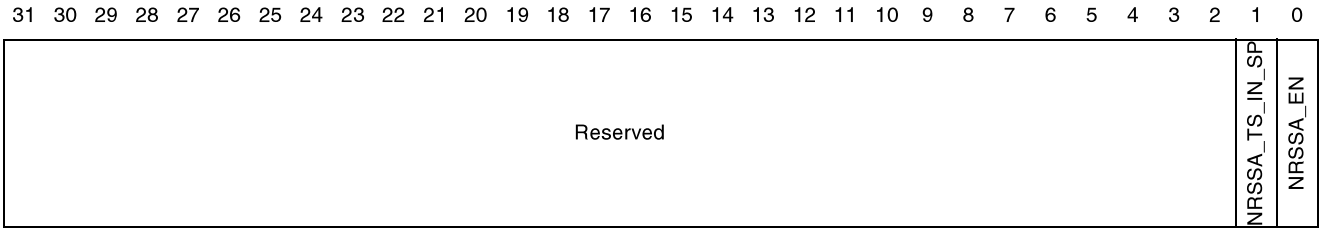
[0] **BYPASS_TS**
0: TS interface is as indicated by TSMerger configuration bits
1: TSIN0 is routed directly to TSOUT1394 output

Figure 58: TSMerger inputs configuration



Note: *See Chapter 38: Transport stream merger and router on page 347.*

SYS_CFG1 System configuration 1: NRSS-A



Address: *SysConfigBaseAddress* + 0x104

Type: R/W

Reset: 0

Description: Configure the NRSS-A interface.

[31:2] **Reserved**

[1] **NRSSA_TS_IN_SP**
0: Bypass mode: TS_IN0 goes directly to the TSmerger
1: NRSS-A interface is enabled: TS_IN0 is formatted and passed through an external NRSS-A module before going to the TSmerger

[0] **NRSSA_EN**
Select TS_IN0 format when NRSS-A is enabled.
0: TS_IN1 in parallel mode
1: TS_IN0 in serial mode

SYS_CFG2 System configuration 2: USB2.0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																						SOFT_JTAG_EN	BYPASS_LFSONLY	MSEL_24_30	SEND_IDLE	RX_EN	TX_EN	LOOP_EN	START_BIST	USB_AT	Reserved

Address: *SysConfigBaseAddress* + 0x108

Type: R/W

Reset: 0x81

Description:

[31:10] **Reserved**

[9] **SOFT_JTAG_EN**
1: USB2 and SATA JTAG are controlled by the SOFT_JTAG register.

[8] **BYPASS_LFSONLY**
0: disables REF_CLK_BYPASS_LFSONLY (PLL outputs are used).
1: REF_CLK_BYPASS_LFSONLY will be used for LFS Serdes operation (in FS and LS only modes). REF_CLK_BYPASS_LFSONLY should be connected to a 48 MHz clock in that case.

[7] **MSEL_24_30**
0: selects a 24MHz input clock.
1: selects a 30 MHz input clock.

[6] **SEND_IDLE**
1: the BIST sends IDLE word on TXN (TXP) signals.

[5] **RX_EN**
1: set the input buffer in normal mode.

[4] **TX_EN**
1: set the output buffer in normal mode.

[3] **LOOP_EN**
1: creates an internal loop between the serializer and the deserializer. This loop is implemented before the buffering stage.

[2] **START_BIST**
1: start the PHY BIST.

[1] **USB_AT**
1: set the USB PHY in self-test mode.

[0] **Reserved**

SYS_CFG3 System configuration 3: video DACs and HDMI

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_S_HDMI_MDIV								PLL_S_HDMI_NDIV								PLL_S_HDMI_PDIV			PLL_S_HDMI_EN	S_HDMI_RST_N	Reserved	TST_DAC_HD_CMDR	TST_DAC_HD_CMDS	TST_DAC_SD_CMDR	TST_DAC_SD_CMDS	DAC_HD_HZU	DAC_HD_HZV	DAC_HD_HZW	DAC_SD_HZU	DAC_SD_HZV	DAC_SD_HZW

Address: *SysConfigBaseAddress* + 0x10C

Type: R/W

Reset: 0x3264 4000

Description: Configure the video DACs and HDMI serializer.

[31:24] **PLL_S_HDMI_MDIV**: Set the dividing factor of the 8-bit programmable input divider

[23:16] **PLL_S_HDMI_NDIV**: Set the dividing factor of the 8-bit programmable loop divider

[15:13] **PLL_S_HDMI_PDIV:** Set the dividing factor of the 3-bit programmable output divider

[12] **PLL_S_HDMI_EN**: Determine the mode of operation of the PLL
0: the PLL is powered down.
1: the PLL is running.

[11] **S_HDMI_RST_N**
0: HDMI serializer reset - active low.

[10] **Reserved**

[9] **TST_DAC_HD_CMDR**
Functions with CMDS signals. Can be used to force DAC HD output.

[8] **TST_DAC_HD_CMDS**
Functions with CMDR signal. Can be used to force DAC HD output.

[7] **TST_DAC_SD_CMDR**
Functions with CMDS signals. Can be used to force the DAC SD output.

[6] **TST_DAC_SD_CMDS**
Functions with CMDR signal. Can be used to force the DAC SD output.

[5] **DAC_HD_HZU**
1: Disable the DAC HD output current and put the output in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

[4] **DAC_HD_HZV**
1: Disable the DAC HD output current and put the output in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

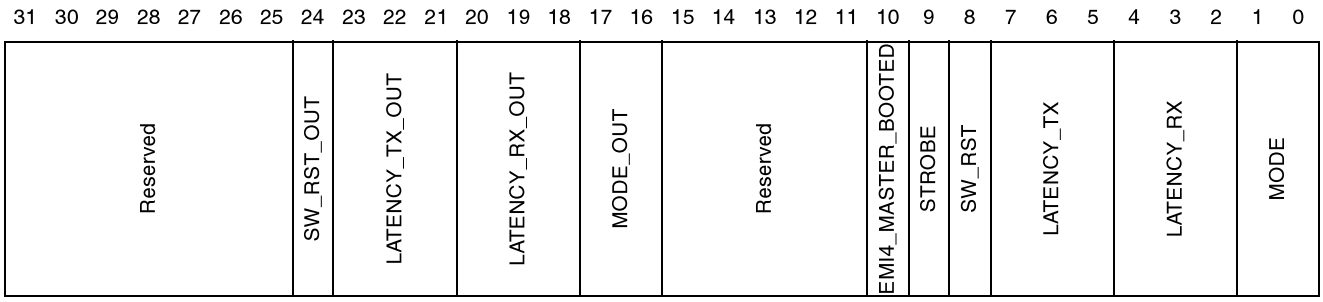
[3] **DAC_HD_HZW**
1: Disable the DAC HD output current and put the output in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

[2] **DAC_SD_HZU**
1: Disable the DAC SD output current and put the output in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

[1] **DAC_SD_HZV**
1: Disable the DAC SD output current and put the output in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

[0] **DAC_SD_HZW**
1: Disable the DAC SD output current and put the output in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

SYS_CFG4 System configuration 4: EMI asynchronous bridge



Address: *SysConfigBaseAddress* + 0x110

Type: Mixed

Reset: 0x0127 0027

Description: Configures the EMI asynchronous bridge.

A rising edge on the strobe signal validates a new bridge configuration. To write a new configuration, the software must write the new configuration (MODE/LATENCY/ SW_RST) while keeping the strobe bit at 0. Setting the strobe bit to 1 creates a rising edge which validates the new setting.

The status of the control bits returned by the bridge can also be read back from this register.

[31:25] - **Reserved**

[24] RO **SW_RST_OUT**: Software reset - active low

[23:21] RO **LATENCY_TX_OUT**: Transmit latency

[20:18] RO **LATENCY_RX_OUT**: Receive latency

[17:16] RO **MODE_OUT**: Mode

[15:11] - **Reserved**

[10] R/W **EMI4_MASTER_BOOTED**
Bit used to gate the request from external slave until the master has completed its boot.

[9] R/W **STROBE**: Strobe to validate a new configuration

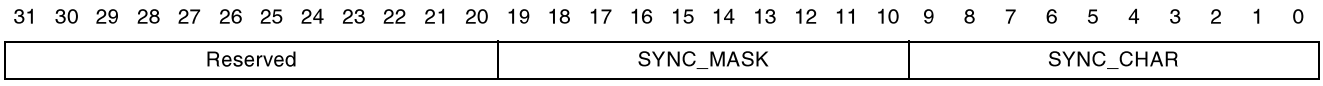
[8] R/W **SW_RST**: Software reset - active high

[7:5] R/W **LATENCY_TX**: Transmit latency value

[4:2] R/W **LATENCY_RX**: Receive latency value

[1:0] R/W **MODE**: Mode pins of memory bridge

SYS_CFG6 System configuration 6: SATA



Address: *SysConfigBaseAddress* + 0x118

Type: R/W

Reset: 0x000F FD7C

Description:

[31:20] **Reserved**

[19:10] **SYNC_MASK**: Defines the 10-bit comma word mask

[9:0] **SYNC_CHAR**: Defines the 10-bit comma word

SYS_CFG7 System configuration 7: PIOs alternate

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																			DAA_SER_EN	AUX_NOT_MAIN	DVO_OUT_ON	IRB_DATA_OUT_POL_OD	SC_DETECT_POL	SC_COND_VCC_EN	Reserved	PIO1_SCCLK_NOT_CLKDSS	PIO0_SCCLK_NOT_CLK_DSS	SSC2_MUX_SEL	SSC1_MUX_SEL	SSC0_MUX_SEL	SCIF_PIO_OUT_EN

Address: *SysConfigBaseAddress* + 0x11C

Type: R/W

Reset: 0

Description: COMMs configuration

[31:13] **Reserved**

[12] **DAA_SER_EN**: DAA serializer enable
0: DAA serializer disable 1: DAA serializer enable

[11] **AUX_NOT_MAIN**: VTG signals selection; see Section 7.2: *Alternative functions on page 54*.

[10] **DVO_OUT_ON**: DVO signals selection; see Section 7.2: *Alternative functions on page 54*.

[9] **IRB_DATA_OUT_POL_OD**: IRB polarity selection
0: Polarity of IRB_DATA_OUT_OD is inverted.
1: IRB_DATA_OUT_OD has same polarity as IRB_DATA_OUT.

[8] **SC_DETECT_POL**: SC_DETECT input signal polarity
When configuration bit SC_COND_VCC_EN is set:
0: output SC_NOT_SETVCC = SC_DETECT.
1: output SC_NOT_SETVCC = NOT(SC_DETECT)
If SC_COND_VCC_EN is 0, then this bit has no effect.

[7] **SC_COND_VCC_EN:** Smartcard VCC control upon detection of smartcard removal or insertion
0: Alternate PIO output pin SC_NOT_SETVCC is controlled according to input SC_DETECT.
1: Alternate PIO output pin SC_NOT_SETVCC is driven permanently low.
This bit is overridden by PDES_SC_MUXOUT which is driven by a configuration bit in the PDES IP

[6] **Reserved**

[5] **PIO1_SCCLK_NOT_CLKDSS**: Smartcard clock muxing selection
0: Smartcard clock sourced from smartcard clock generator (COMMs): SC_CLKGEN1_CLK_OUT.
1: Smartcard clock sourced from CLK_DSS (clockgen B).

[4] **PIO0_SCCLK_NOT_CLK_DSS**: Smartcard clock muxing selection
0: Smartcard clock sourced from CLK_DSS (clockgen B).
1: Smartcard clock sourced from smartcard clock generator (COMMs): SC_CLKGEN0_CLK_OUT.

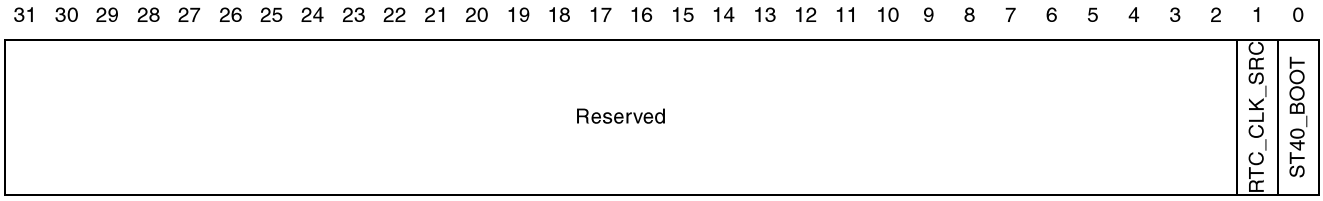
[3] **SSC2_MUX_SEL**: SSC2 muxing selection; see Section 7.2: *Alternative functions on page 54*.
0: On separate PIOs.
1: SSC0_MRST replaces SSC0_MTSR on the corresponding PIO alternate function.

[2] **SSC1_MUX_SEL**: SSC1 muxing selection; see Section 7.2: *Alternative functions on page 54*.
0: Default assignment
1: SSC0_MRST replaces SSC0_MTSR on the corresponding PIO alternate function.

[1] **SSC0_MUX_SEL**: SSC0 muxing selection; see Section 7.2: *Alternative functions on page 54*.
0: Default assignment
1: SSC0_MRST replaces SSC0_MTSR on the corresponding PIO alternate function.

[0] **SCIF_PIO_OUT_EN**
0: Regular PIO 1: Select the SCIF output

SYS_CFG8 System configuration 8: ST40 boot control



Address: *SysConfigBaseAddress* + 0x120

Type: R/W

Reset: 1 when mode[12:11]=00, otherwise 0

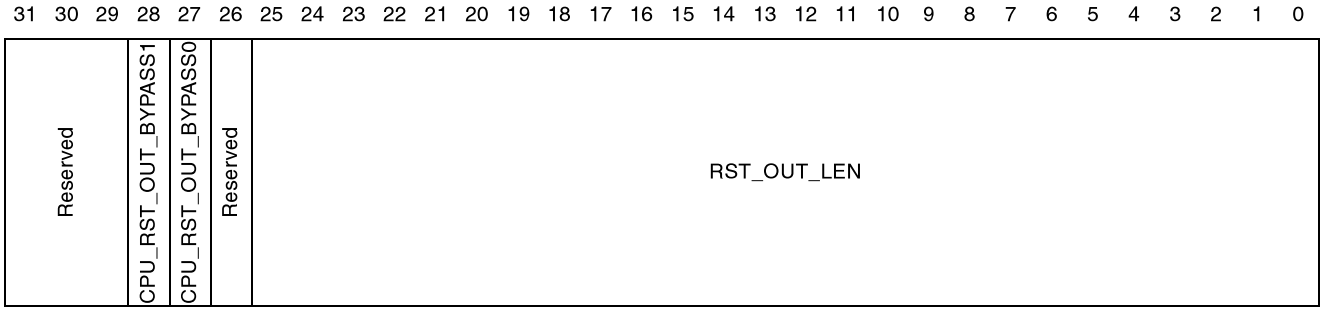
Description:

[31:2] **Reserved**

[1] **RTC_CLK_SRC**: RTC clock source
0: The ST40 RTC sources its clock from the input pin RTCCLKIN
1: The ST40 RTC sources its clock from clock generator B (fixed frequency 32.768 kHz)

[0] **ST40_BOOT**: Controls whether the ST40 is allowed to boot or not after a reset. Its value depends on the mode pin [12] captured during the reset phase.
0: Boot halted 1: Boot enabled

SYS_CFG9 System configuration 9: reset generator



Address: *SysConfigBaseAddress* + 0x124

Type: R/W

Reset: See below

Description: Configures the reset generator.

[31:29] **Reserved**

[28] **CPU_RST_OUT_BYPASS1**: CPU reset out bypass 1
0: The reset signal is propagated through the ST231.
1: Bypass the audio ST231 and Delta ST231 reset out signals.
Reset: from mode pin [5].

[27] **CPU_RST_OUT_BYPASS0**: CPU reset out bypass 0
0: The reset signal is propagated through the ST231s and the ST40
1: Bypass the ST40, Audio ST231 and Delta ST231 reset out signals.
Reset: from mode pin [4].

[26] **Reserved**

[25:0] **RST_OUT_LEN**: Length of WDGRTS_OUT in 27 MHz cycles
In long reset out mode, the reset value guarantees a 200 ms WDGRTS_OUT signal.
In short reset out mode, the WDGRTS_OUT signal lasts 100 µs.
This register allows for a max reset out of 2.48 sec.
Reset: 0x52 65C0 in long reset out mode[a], 0x00 0A8C in short reset out mode

a. Long reset out mode is selected when MODE_PIN[13] is set to '1'.

SYS_CFG10 System configuration 10: SYS_IRQ pins

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												SYS_IRQ3_DIR	SYS_IRQ2_DIR	SYS_IRQ1_DIR	SYS_IRQ0_DIR

Address: *SysConfigBaseAddress* + 0x128

Type: R/W

Reset: 0xF

Description: Configure the SYSITRQ pins as either input or output.

[31:4] **Reserved**

[3] **SYS_IRQ3_DIR**: SYSITRQ3 pin direction
0: SYSITRQ3 configured as output
1: SYSITRQ3 configured as input.

[2] **SYS_IRQ2_DIR**: SYSITRQ2 pin direction
0: SYSITRQ2 configured as output.
1: SYSITRQ2 configured as input.

[1] **SYS_IRQ1_DIR**: SYSITRQ1 pin direction
0: SYSITRQ1 configured as output.
1: SYSITRQ1 configured as input.

[0] **SYS_IRQ0_DIR**: SYSITRQ0 pin direction
0: SYSITRQ0 configured as output.
1: SYSITRQ0 configured as input.

SYS_CFG11 System configuration 11: system and video padlogic

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	LMI_VID_PWR_DN_REQ	Reserved	LMI_SYS_PWRD_REQ	BYPASS_DQS_EN	LMI_VID_SWAP_ADD_13_11	LMI_VID_SWAP_ADD_13_10	LMI_SYS_SWAP_ADD_13_11	LMI_SYS_SWAP_ADD_13_10	LMI_VID_HP_AP_EN	LMI_VID_LP_AP_EN	LMI_SYS_HP_AP_EN	LMI_SYS_LP_AP_EN	LMI_VID_PL_RETIME	LMI_SYS_PL_RETIME	LMI_VID_CKG_RSTN	LMI_VID_RST_N	LMI_VID_PBS_IN							Reserved	LMI_SYS_CKG_RSTN	LMI_SYS_RST_N	LMI_SYS_PBS_IN					

Address: *SysConfigBaseAddress* + 0x012C

Type: R/W

Reset: 0x0800 0000

Description: Controls the configuration of the system and video LMI padlogics, reset of the system, video memory controllers and their padlogics. Can also put the memory controllers in power-down mode.

[31] **Reserved**

[30] **LMI_VID_PWR_DN_REQ**: Video LMI - power down request

[29] **Reserved**

[28] **LMI_SYS_PWRD_REQ**: System LMI - power down request

[27] **BYPASS_DQS_EN**
Bypass gating logic for DQS strobe during postamble. Must be set to 1.

[26] **LMI_VID_SWAP_ADD_13_11**
Video LMI - Enable swapping between bit 13 and bit 11 of STBus address.

[25] **LMI_VID_SWAP_ADD_13_10**
Video LMI - Enable swapping between bit 13 and bit 10 of STBus address.

[24] **LMI_SYS_SWAP_ADD_13_11**
System LMI - Enable swapping between bit 13 and bit 11 of STBus address.

[23] **LMI_SYS_SWAP_ADD_13_10**
System LMI - Enable swapping between bit 13 and bit 10 of STBus address.

[22] **LMI_VID_HP_AP_EN**
Video LMI - Enable read with autoprecharge on high priority port.

[21] **LMI_VID_LP_AP_EN**
Video LMI - Enable read with autoprecharge on low priority port.

[20] **LMI_SYS_HP_AP_EN**
System LMI - Enable read with autoprecharge on high priority port.

[19] **LMI_SYS_LP_AP_EN**
System LMI - Enable read with autoprecharge on low priority port.

[18] **LMI_VID_PL_RETIME**
Video LMI - retiming stage enable. Active high

[17] **LMI_SYS_PL_RETIME**: System LMI - retiming stage enable. Active high

[16] **LMI_VID_CKG_RSTN**: Video LMI - padlogic clockgen reset. Active low.

[15] **LMI_VID_RST_N**: Video LMI - subsystem reset and padlogic reset. Active low.

[14:9] **LMI_VID_PBS_IN**: Video LMI - padlogic pin buffer strength.
Set the output buffer drive strength for the SSTL2 pads. Each 2-bits control field has the following encoding:
00: 5 pf 01: 15 pf
10: 25 pf 11: 35 pf
[10:9]: Clock buffer strength. This field selects the drive strength for the CK and CK# pins.
[12:11]: Command buffer strength. This field selects the drive strength for the CKE, CS, RAS, CAS, WE, A and BA DDR pins.
[14:13]: Data buffer strength. This field selects the drive strength for the DQ, DM and DQS DDR pins.

[8] **Reserved**

[7] **LMI_SYS_CKG_RSTN**: System LMI - padlogic clockgen reset. Active low

[6] **LMI_SYS_RST_N**: System LMI - subsystem reset and padlogic reset. Active low.

[5:0] **LMI_SYS_PBS_IN**: System LMI - padlogic pin buffer strength
Set the output buffer drive strength for the SSTL2 pads. Each 2-bit control field has the following encoding:
00: 5 pf 01: 15 pf
10: 25 pf 11: 35 pf
[1:0]: Clock buffer strength. This field select the drive strength for the CK and CK# pins.
[3:2]: Command buffer strength. This field selects the drive strength for the CKE, CS, RAS, CAS, WE, A and BA DDR pins.
[5:4]: Data buffer strength. This field selects the drive strength for the DQ, DM and DQS DDR pins.

SYS_CFG12 System configuration 12: LMI padlogic

31	30	29	28	27	26 25 24	23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
LMI_SYS_IOREF_TQ	LMI_SYS_IOREF_ACC	LMI_SYS_IOREF_FRZ	LMI_SYS_IOREF_COMPTQ	LMI_SYS_IOREF_COMP	LMI_SYS_DLL2_LCK_CTRL	LMI_SYS_IOREF_RASRC	LMI_SYS_DLL1_LCK_CTRL	Reserved	LMI_SYS_DDR_CTRL

Address: *SysConfigBaseAddress* + 0x130

Type: R/W

Reset: 0x4000 0XXD

Description: Control the system LMI DDR padlogic. The drive of the SSTL2 pads, the padlogic DLLs (DLL1 and DLL2) and the compensation cell parameters can be controlled.

[31] **LMI_SYS_IOREF_TQ**: Compensation cell IDDQ mode select
Must be 0 in normal mode
1: puts all IOs and reference generators in IDDQ mode

[30] **LMI_SYS_IOREF_ACC**
Compensation cell accurate mode select (use an external resistor to provide an accurate compensation code). Must be 1 in normal mode.

[29] **LMI_SYS_IOREF_FRZ**: Compensation cell code freeze
Must be 0 in normal mode.
1: Freezes the compensation code at its running value.

[28] **LMI_SYS_IOREF_COMPTQ**: Compensation cell operating mode
Must be 0 in normal mode.

[27] **LMI_SYS_IOREF_COMP**: Compensation cell operating mode
Must be 0 in normal mode.

[26:23] **LMI_SYS_DLL2_LCK_CTRL**: DLL2 lock control
Defines the number of consecutive up/down pulses to trigger the lock status (LCK goes high).

[22:16] **LMI_SYS_IOREF_RASRC**: System LMI compensation cell input code

[15:12] **LMI_SYS_DLL1_LCK_CTRL**: DLL1 lock control
Defines the number of consecutive up/down pulses trigger the lock status (LCK goes high).

[11:4] **Reserved**

[3:0] **LMI_SYS_DDR_CTRL**: System LMI DDR Pad control:
[0] Output buffer impedance (I/O ZOUTPROGA)
0: 25 Ω (Strong SSTL2) 1: 40 Ω (Weak SSTL2)
[1] Buffer mode select (I/O MODE)
0: 2.5V SSTL2 with 25/40 Ω impedance. 1: 2.5V Matched impedance with 40 Ω
[2] VREF mode select (I/O ENVREF)
0: VREF is generated internally for each pad. 1: VREF is supplied externally.
[3]: Receiver mode select (I/O MODEZI)
0: Differential 2.5V receiver. 1: 2.5V Digital CMOS receiver.

SYS_CFG13 System configuration 13: video LMI padlogic

31	30	29	28	27	26 25 24 23	22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
LMI_VID_IOREF_TQ	LMI_VID_IOREF_ACC	LMI_VID_IOREF_FRZ	LMI_VID_IOREF_COMPTQ	LMI_VID_IOREF_COMP	LMI_VID_DLL2_LCK_CTRL	LMI_VID_IOREF_RASRC	LMI_VID_DLL1_LCK_CTRL	Reserved	LMI_VID_DDR_CTRL

Address: *SysConfigBaseAddress* + 0x134

Type: R/W

Reset: 0x4000 0XXD

Description: Control the video LMI DDR padlogic. The drive of the SSTL2 pads, the padlogic DLLs (DLL1 and DLL2) and the compensation cell parameters can be controlled.

[31] **LMI_VID_IOREF_TQ**: Compensation cell IDDQ mode select
Must be 0 in normal mode.

[30] **LMI_VID_IOREF_ACC**: Compensation cell accurate mode select
Must be 1 in normal mode.

[29] **LMI_VID_IOREF_FRZ**: Compensation cell code freeze
Must be 0 in normal mode.

[28] **LMI_VID_IOREF_COMPTQ**: Compensation cell operating mode
Must be 0 in normal mode.

[27] **LMI_VID_IOREF_COMP**: Compensation cell operating mode
Must be 0 in normal mode.

[26:23] **LMI_VID_DLL2_LCK_CTRL**: DLL2 lock control
Defines the number of consecutive up/down pulses trigger the lock status (LCK goes high).

[22:16] **LMI_VID_IOREF_RASRC**: Compensation cell input code

[15:12] **LMI_VID_DLL1_LCK_CTRL**: DLL1 lock control
Defines the number of consecutive up/down pulses trigger the lock status (LCK goes high).

[11:4] **Reserved**

[3:0] **LMI_VID_DDR_CTRL**: Video LMI DDR pad control

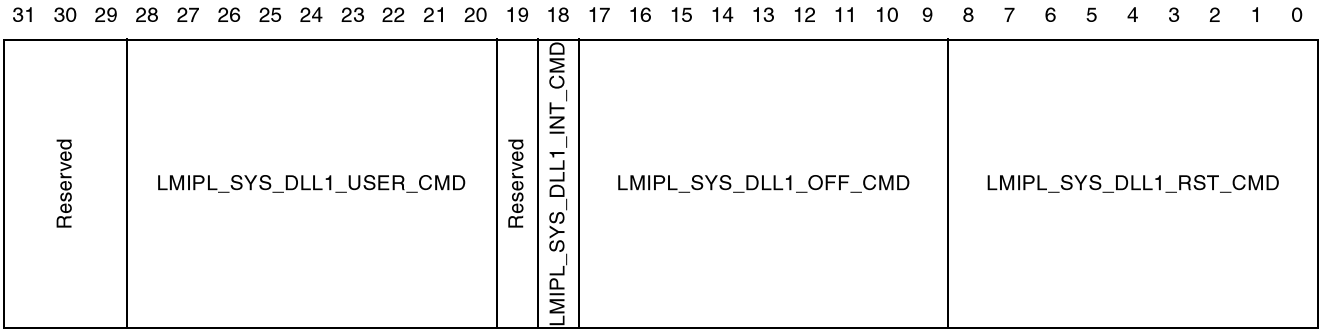
[3] **Receiver mode select** (I/O MODEZI)
0: Differential 2.5V receiver. 1: 2.5V Digital CMOS receiver

[2] **VREF mode select** (I/O ENVREF)
0: VREF is generated internally for each pad. 1: VREF is supplied externally

[1] **Buffer mode select** (I/O MODE)
0: 2.5V SSTL2 with 25/40 Ω impedance. 1: 2.5V Matched impedance with 40 Ω

[0] **Output buffer impedance** (I/O ZOUTPROGA)
0: 25 Ω (Strong SSTL2) 1: 40 Ω (Weak SSTL2)

SYS_CFG14 System configuration 14: LMI padlogic DLL1



Address: *SysConfigBaseAddress* + 0x138

Type: R/W

Reset: 0

Description: Controls the delay generated by the DLL1 of the system LMI padlogic. The DLL1 generates only internal delay commands. It controls the timings of the write-path to the DDR memory.

[31:29] **Reserved**

[28:20] **LMIPL_SYS_DLL1_USER_CMD**
User delay command used by DLL1 when bit 18 is 1.

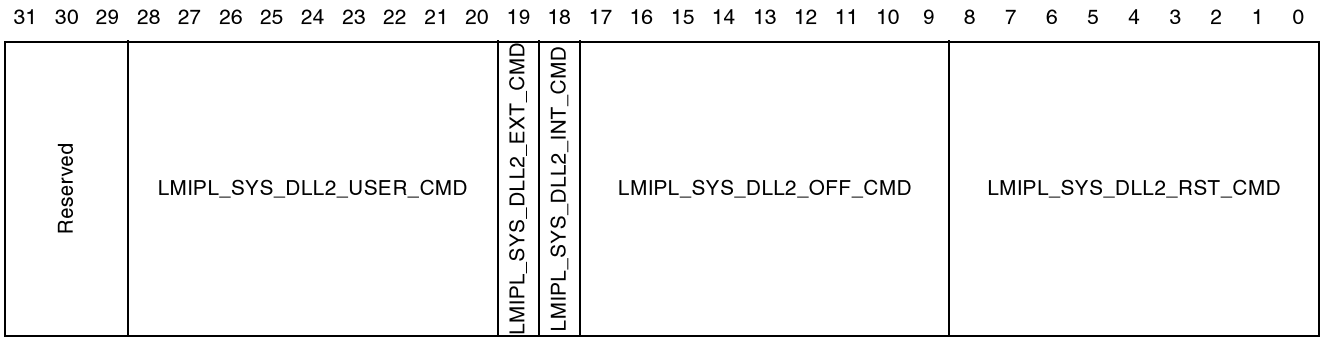
[19] **Reserved**

[18] **LMIPL_SYS_DLL1_INT_CMD**: Controls which internal delay command is used by DLL1
0: FSM-generated command
1: user command

[17:9] **LMIPL_SYS_DLL1_OFF_CMD**
DLL1 offset value added to the FSM generated delay command. Can be negative and must be coded in twos complement.

[8:0] **LMIPL_SYS_DLL1_RST_CMD**
DLL1 command from which the FSM start to count-up after reset.

SYS_CFG15 System configuration 15: LMI padlogic DLL2



Address: *SysConfigBaseAddress* + 0x13C

Type: R/W

Reset: 0

Description: Controls the delay generated by the DLL2 of the system LMI padlogic. The DLL2 delay can be generated by either internal and external commands. This delay from the DLL2 is used to control the read-path timings the from the DDR memory.

[31:29] **Reserved**

[28:20] **LMIPL_SYS_DLL2_USER_CMD**: User delay command used by DLL2 when bit 18 and/or bit 19 is 1

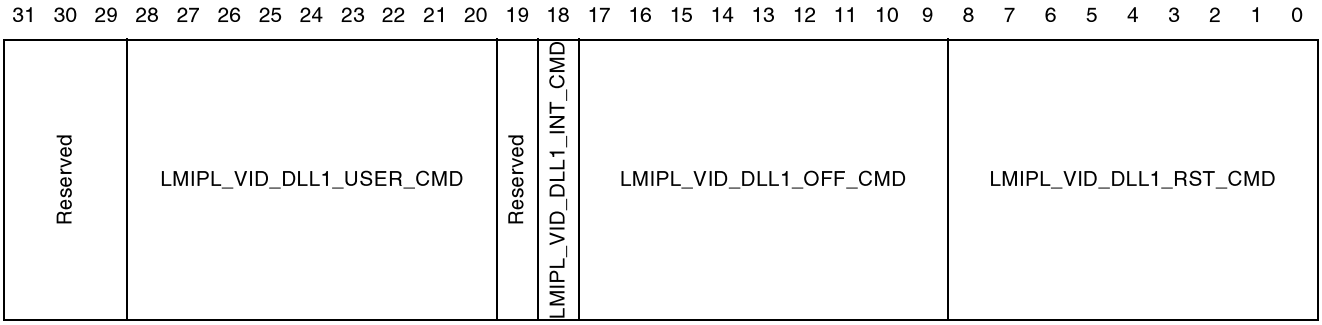
[19] **LMIPL_SYS_DLL2_EXT_CMD**: Controls which external delay command is used for DLL2
0: FSM-generated delay command
1: user external delay command

[18] **LMIPL_SYS_DLL2_INT_CMD**: Controls which internal delay command is used for DLL2
0: FSM-generated delay command
1: user internal delay command

[17:9] **LMIPL_SYS_DLL2_OFF_CMD**: DLL2 offset value added to the FSM generated delay command
Can be negative and must be coded in 2's complement.

[8:0] **LMIPL_SYS_DLL2_RST_CMD**: DLL2 command from which the FSM start to count-up after reset

SYS_CFG20 System configuration 20: video LMI padlogic DLL1



Address: *SysConfigBaseAddress* + 0x150

Type: R/W

Reset: 0

Description: Controls the delay generated by the DLL1 of the video LMI padlogic and the timings of the write-path to the DDR memory. The DLL1 generates only internal delay commands. controls.

[31:29] **Reserved**

[28:20] **LMIPL_VID_DLL1_USER_CMD**: User delay command used by DLL1 when the bit 18 is 1.

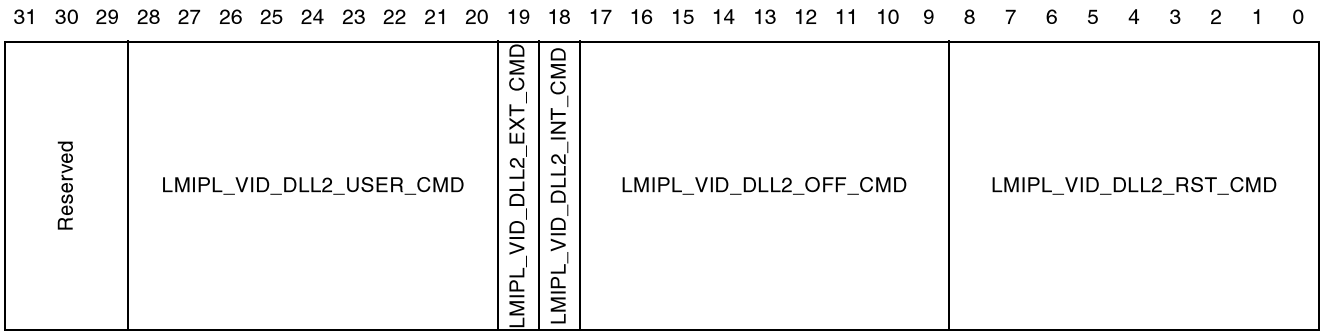
[19] **Reserved**

[18] **LMIPL_VID_DLL1_INT_CMD**: Controls which internal delay command is used by DLL1
0: FSM-generated command
1: user command

[17:9] **LMIPL_VID_DLL1_OFF_CMD**
DLL1 offset value added to the FSM generated delay command. Can be negative and must be coded in 2's complement.

[8:0] **LMIPL_VID_DLL1_RST_CMD**: DLL1 command from which the FSM start to count-up after reset.

SYS_CFG21 System configuration 21: video LMI padlogic DLL2



Address: *SysConfigBaseAddress* + 0x154

Type: R/W

Reset: 0

Description: Controls the delay generated by the DLL2 of the system LMI padlogic and timings of the read-path from the DDR memory. The DLL2 generates internal and external delay commands.

[31:29] **Reserved**

[28:20] **LMIPL_VID_DLL2_USER_CMD**
User delay command used by DLL2 when bit 18 and/or bit 19 is 1

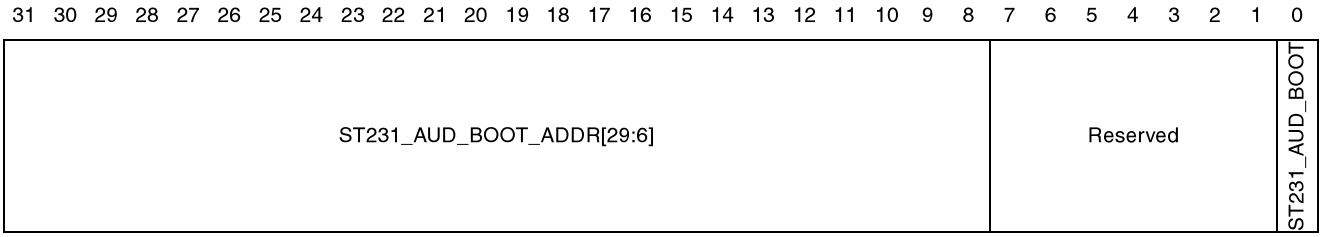
[19] **LMIPL_VID_DLL2_EXT_CMD**
Controls which external delay command is used for DLL2.
0: FSM-generated delay command
1: user external delay command

[18] **LMIPL_VID_DLL2_INT_CMD**
Controls which internal delay command is used for DLL2.
0: FSM-generated delay command
1: user internal delay command

[17:9] **LMIPL_VID_DLL2_OFF_CMD**
DLL2 offset value added to the FSM generated delay command. Can be negative and must be coded in 2's complement.

[8:0] **LMIPL_VID_DLL2_RST_CMD**
DLL2 command from which the FSM start to count-up after reset.

SYS_CFG26 System configuration 26: audio ST231 boot control



Address: *SysConfigBaseAddress* + 0x

Type: R/W

Reset: 0

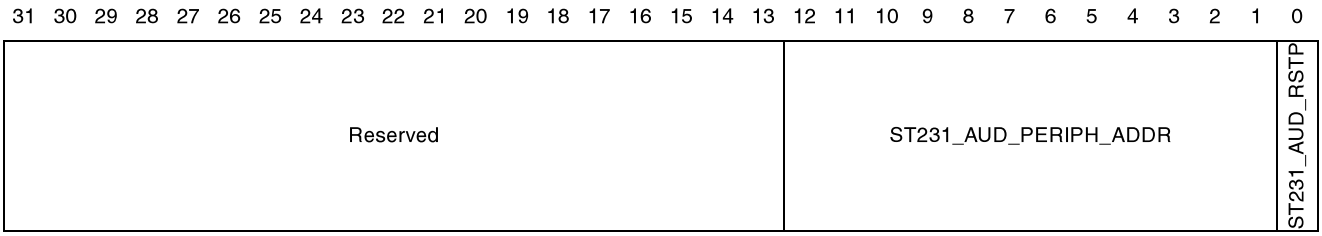
Description: Allows the audio ST231 to boot and to define its boot address.

[31:8] **ST231_AUD_BOOT_ADDR**[29:6]: Audio ST231 boot address

[7:1] **Reserved**

[0] **ST231_AUD_BOOT**: Audio ST231 boot enable
0: boot halted
1: boot enabled

SYS_CFG27 System configuration 27: audio ST231 reset



Address: *SysConfigBaseAddress* + 0x1C

Type: R/W

Reset: 0x344

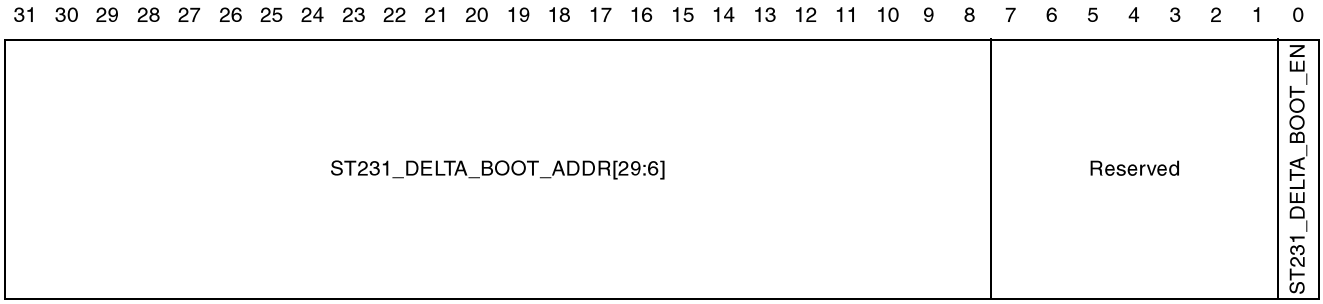
Description: do a software reset of the audio ST231. When the boot-address is changed then the ST231 must be reset to take into account its new boot-address.

[31:13] **Reserved**

[12:1] **ST231_AUD_PERIPH_ADDR**: Audio ST231 peripherals address (must not be changed).

[0] **ST231_AUD_RSTP**: Audio ST231 reset control:
0: ST231 reset input is driven by the hardware reset
1: ST231 reset is asserted

SYS_CFG28 System configuration 28: Delta ST231 boot



Address: *SysConfigBaseAddress* + 0x170

Type: R/W

Reset: 0

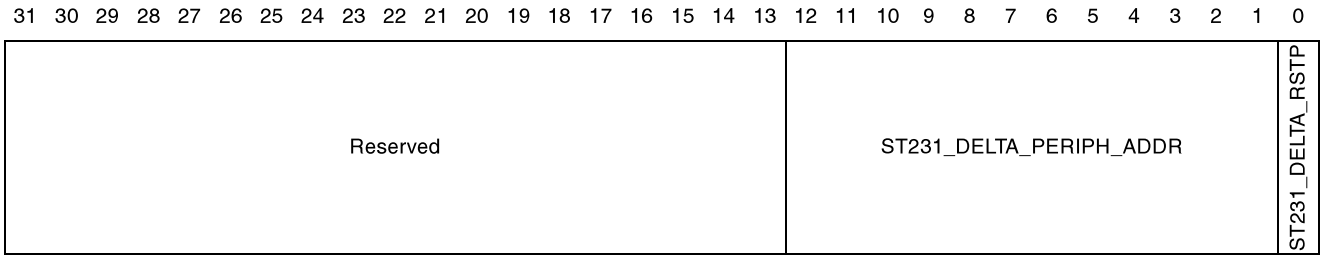
Description: Enables the Delta ST231 to boot and defines its boot address.

[31:8] **ST231_DELTA_BOOT_ADDR**[29:6]

[7:1] **Reserved**

[0] **ST231_DELTA_BOOT_EN**: Delta ST231 boot enable
0: Boot halted
1: Boot enabled

SYS_CFG29 System configuration 29: Delta ST231 reset



Address: *SysConfigBaseAddress* + 0x174

Type: R/W

Reset: 0x340

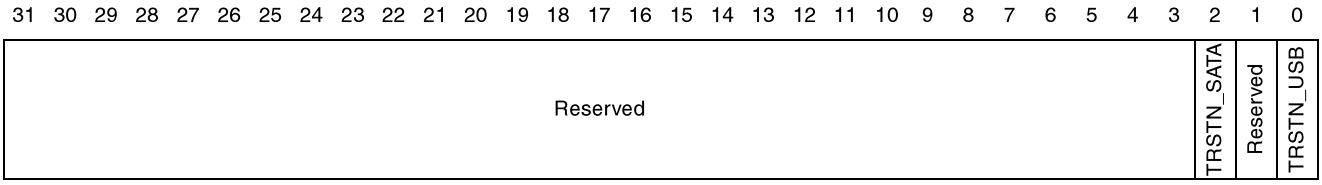
Description: Perform a software reset of the Delta ST231. When the boot-address is changed then the ST231 must be reset to take into account its new boot address.

[31:13] **Reserved**

[12:1] **ST231_DELTA_PERIPH_ADDR**: Delta ST231 peripherals address (must not be changed).

[0] **ST231_DELTA_RSTP**: Delta ST231 reset control:
0: ST231 reset input is driven by the hardware reset
1: ST231 reset is asserted

SYS_CFG33 System configuration 33: USB and SATA software JTAG



Address: *SysConfigBaseAddress* + 0x184

Type: R/W

Reset: 0

Description: Controls the JTAG port of the SATA and USB PHY. A software JTAG controller can be implemented in software.

[31:3] **Reserved**

[2] **TRSTN_SATA**: Asynchronous reset SATA TAP

[1] **Reserved**

[0] **TRSTN_USB**: Asynchronous reset USB2 TAP

22 Interrupt system

The STx7100 has two interrupt networks. One is associated with the ST40 CPU and the other is associated with the Delta (H.264) ST231 CPU when it used as an application processor. The interrupt lines are routed to both the ST40 and the Delta ST231. For both processors, it is up to software to handle the interrupts.

22.1 ST40 Interrupt network

22.1.1 Internal and external interrupts

The ST40 CPU has two types of interrupts:

External Interrupts

- NMI (Non-Maskable Interrupt): External interrupt source.
- SYSITRQ(3-0): 4 external interrupt sources SYSITRQ(3-0) which can be configured as 4 independent interrupts or encoded to provide 15 external interrupt levels.

These interrupts are managed by the INTC2 interrupt controller integrated into the ST40 CPU core.

Internal Peripherals Interrupts

- ST40-P130 peripherals interrupts:
  - UDI (user debug interface)
  - TMU0, 1 (timer unit)
  - RTC (real time clock)
  - SCIF (serial controller interface)

  These interrupts are controlled by the interrupt controller INTC2, and expansion of the INTC. All interrupts are assigned a priority level between 0 and 15: level 15 is the highest and level 1 the lowest, level 0 means that the interrupt is masked. The NMI is defined to have a fixed priority level of 16.
- On-chip peripherals interrupts

  These interrupts are managed by the INTC2 (interrupt controller).

  The INTC2 accepts 16 groups of 4 interrupts (64 total); each group can be assigned a priority by software (INTPRI*xx* registers). Within each group (of 4 interrupts), there is a fixed priority, with interrupt 4 having the highest priority. All interrupts are resynchronized in INTC2.

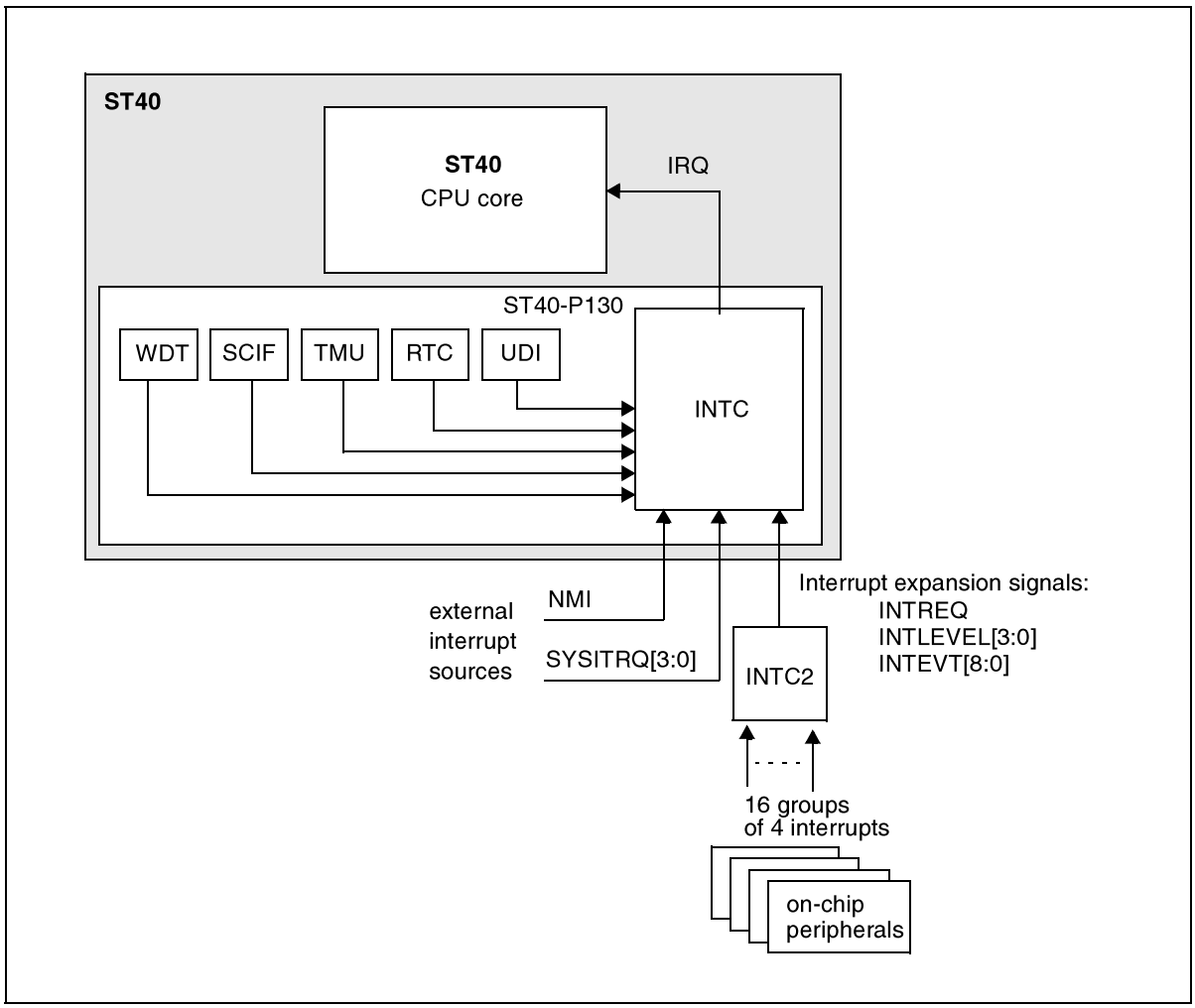
22.1.2 Interrupt service routine address

Whenever an interrupt occurs, the ST40 CPU branches to the interrupt handling vector address determined by adding the fixed offset 0x600 to the vector base address (VBR) register. Each interrupt type is assigned a code which is stored in the INTEVT (interrupt event) register when the interrupt occurs. This enables the interrupt service routine to identify the interrupt source type.

The interrupt controller is responsible for mapping each interrupt to its code (INTEVT).

Figure 59 shows the ST40 interrupt network, and Table 83: *ST40 on-chip peripheral interrupts on page 201* lists the internal interrupts with their INTEVT code.

Figure 59: ST40 interrupt network



22.1.3 INTC2 secondary interrupt controller

The INTC2 selects the highest priority, unmasked interrupt from all of its interrupt inputs, and passes the INTEVT code of this interrupt to the INTC2 for further processing.

The INTC2 allows interrupts to be grouped together. These groups contain one or more interrupts. For each interrupt within a group, and for each group, the INTC2 provides the following:

Each interrupt group is allocated a four-bit section of the INTC2_PRI0*n* register. This gives the group its overall interrupt priority. Within each group, each individual interrupt has its own priority. (By setting a group's priority to 0x0, the whole group can be masked).

Each interrupt is allocated a single bit of the INTC2_REQ0*n* and INTC2_MSK0*n* registers. Register INTC2_REQ0*n* shows the status of an individual interrupt request signal irrespective of the state of register INTC2_MSK0*n*. The INTC2_MSK0*n* register allows each individual interrupt to be separately masked.

Each priority group of interrupts asserts its highest priority interrupt. A tree structure is used to compare all asserted interrupts to determine the highest priority interrupt, which is then passed to the INTC. The INTEVT code which is sent to the INTC.

22.2 Delta (H.264) ST231 interrupt network

The ST231 accepts 60 external interrupts (from 63 to 3). Interrupts 0 to 2 are reserved for the ST231 internal timers. All the interrupts are maskable but with a single level of priority. Multiple level priority must be implemented in software.

Table 85: *Delta ST231 Interrupts* *on page 204* describes the mapping of the interrupts on the ST231 interrupt controller.

When used as an application processor, the Delta ST231 processor receives the same internal interrupts than the ST40 processor except the interrupts generated by the Delta coprocessors (CABAC preprocessor 1 and 2).

The Delta ST231 receives also the external interrupts via the ILC interrupt controller.

22.3 STx7100 interrupt network

ILC interrupt level controller

The STx7100 interrupt network includes an ILC interrupt level controller. The ILC accepts 64 synchronous interrupt inputs (the on-chip peripherals interrupts) and six asynchronous interrupt inputs (the 4 external interrupts SYSITRQ(3-0), NMI and the IRB wake-up interrupt). The external asynchronous interrupts can have up to 5 programmable triggering conditions (active high, active low, falling edge, rising edge or any edge).

The ILC can map any of the synchronous internal interrupts and asynchronous interrupts onto a group of 8 internal interrupts ILC_EXT_OUT(7-0).

The interrupts ILC_EXT_OUT(3-0) can be used as external interrupt outputs through the SYSITRQ(3-0) pins.

The interrupts ILC_EXT_OUT(7-4) are routed to the ST40 interrupts IRL(3-0).

The ILC mapping is described in Table 86: *ILC interrupt mapping* *on page 206*.

Wake up by Interrupt

The ILC has also an interrupt output dedicated to the wake-up process that is used by the low power controller. A pulse stretcher receives a transition from the UHF and IR input pins and generates an interrupt that can be routed through the ILC to one of the ILC_EXT_OUT(7-4) interrupt lines and used as a wake-up interrupt to the ST40 (for details, see Chapter 18: *Low-power modes* *on page 164*).

Internal peripheral interrupts

Both the ST40 and the Delta ST231 receive all the internal interrupt requests. It is up to the software to define the CPU that will serve each interrupt request.

All the internal interrupts are routed to the INTC2, ST231 Interrupt controller and ILC. All the internal interrupts are level sensitive and active high.

External interrupts inputs

The four external asynchronous interrupts are routed to the ILC interrupt controller before reaching the ST40 and ST231 in order to synchronize and change the polarity if needed. The ST40 expects the interrupts to be active high. These interrupts are then output from the ILC (ILC_EXT_OUT(7-4)) to be routed toward the ST40 and Delta ST231.

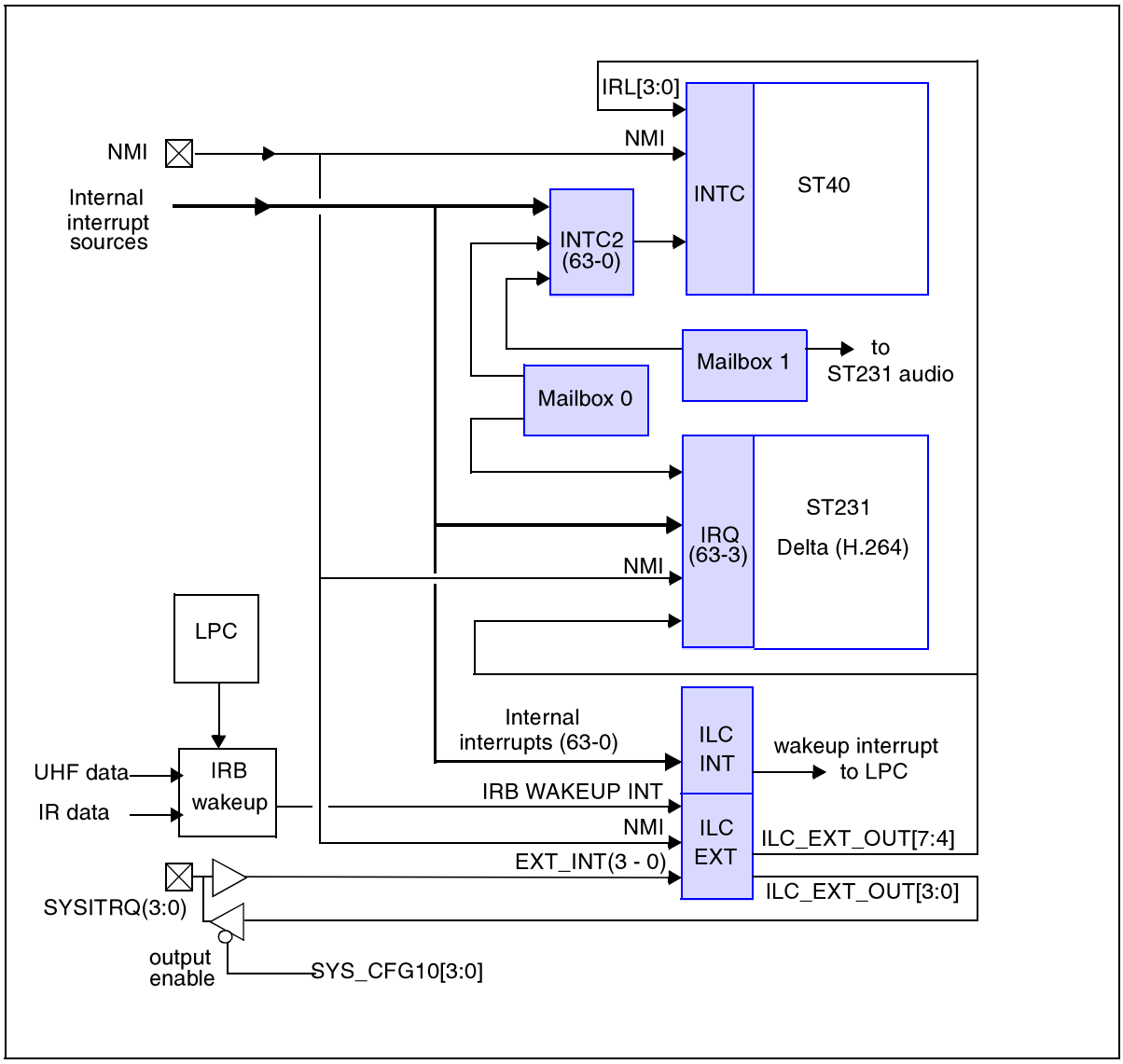
External interrupts outputs

The ILC has the capability to output a subset of the interrupts that are connected to it. Four of these interrupts (ILC_EXT_OUT[3 - 0]) are software selectable to be output externally for remote devices.

Control of the external interrupts direction

The direction of external interrupts is controlled by the configuration register SYS_CFG10[3:0]. By default, pins SYSITRQ(3-0) are configured as inputs (SYS_CFG10 bits set to logic 1). Setting these bits to 0 configures the pins as outputs.

Figure 60: STx7100 interrupt network



23 Interrupt maps

This chapter contains Interrupt mapping tables for the:

- ST40,
- INTC2
- Delta (H.264) ST231,
- STx7100 ILC.

23.1 ST40 interrupts

Table 82: ST40 P130 interrupts

Interrupt source		INTEVT code	IPR (bit numbers)	Interrupt priority (initial value)
NMI		0x1C0	-	16
IRL independent encoding	IRL0	0x240	IPRD[15:12]	15-0 (13)
	IRL1	0x2A0	IPRD[11:8]	15-0 (10)
	IRL2	0x300	IPRD[7:4]	15-0 (7)
	IRL3	0x360	IPRD[3:0]	15-0 (4)
IRL	level encoding	0x200 - 0x3C0	-	1-15
TMU0	TUNI0	0x400	IPRA[15:12]	15-0 (0)
TMU1	TUNI1	0x420	IPRA[11:8]	15-0 (0)
TMU2	TUNI2	0x440	IPRA[7:4]	15-0 (0)
	TICPI2	0x460		
RTC	ATI	0x480	IPRA[3:0]	15-0 (0)
	PRI	0x4A0		
	CUI	0x4C0		
SCIF	ERI	0x4E0	IPRB[7:4]	15-0 (0)
	RXI	0x500		
	BRI	0x520		
	TXI	0x540		
WDT	ITI	0x560	IPRB[15:12]	15-0 (0)
UDI	H-UDI	0x600	IPRC[3:0]	15-0 (0)